Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(EIE-OLD)/SEM-4/CS-404(EI)/2012

2012

COMPUTER ORGANIZATION & ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) CPU consists of
      a) main memory and ALU
      b) main memory, ALU and control unit
      c) cache memory, ALU and control unit
      d) ALU, control unit and registers.

   ii) The minimum and maximum 8-bit numbers in sign magnitude representation are
      a) 0 and 255 b) – 127 and 127
      c) – 128 and 127 d) none of these.

   iii) Cache memory
      a) increases performance
      b) increases machine cycle
      c) reduces performance
      d) none of these.

iv) How many address bits are required for a 1024 × 8 memory ?

a) 1024 b) 5

c) 10 d) None of these.

v) Which logic gate has the highest speed ?

a) DTL b) ECL

c) RTL d) TTL.

vi) Instruction cycle is

a) fetch — decode — execution

b) fetch — execution — decode

c) decode — fetch — execution

d) none of these.

vii) The basic principle of the von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large number of registers.

viii) The technique of placing software in a ROM semiconductor chip is called

a) PROM b) EPROM

c) FIRMWARE d) Microprocessor.

ix) The maximum unsigned binary number in 8 bit is

a) 255 b) 256

c) 128 d) 127.

x) The conversion of $(FAFAFA)_{16}$ into octal form is

a) 76767676 b) 76575372

c) 76737672 d) 76727672.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is virtual memory ? Why is it called virtual ? Write the advantage of virtual memory. 2 + 1 + 2
3. Why does Dynamic MOS cell need periodic refreshing ? What is the role of an operating system ? 3 + 2
4. a) Write + $8{\cdot}75_{10}$ in IEEE 32-bit format.
   b) Convert IEEE 32-bit format 40400000_{16} in decimal value. 3 + 2
5. What is von Neumann architecture ? What is von Neumann bottleneck ? 3 + 2
6. Compare sequential circuit with combinational circuit. What is the necessity of guard bits ? 4 + 1

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Give the Booth's algorithm for multiplication of signed 2's complement numbers in flowchart and explain.
   b) Multiply – 7 by + 5 using Booth's algorithm. (Take 5-bit for operation)
   c) Compare Restoring division algorithm with Non-restoring division algorithm with an example and flowchart. 3 + 5 + 7
8. a) Describe the function of major components of a digital computer with neat sketch.
   b) Explain the reading and writing operations of a basic static MOS cell.
   c) Describe the two 'write' policies for the cache design. What are the advantages and disadvantages of both methods ? 5 + 5 + 5

9. a) What will be the maximum capacity of a memory which uses an address bus of size 12 bit ?

   b) What is an instruction format ? What is instruction cycle ? Draw the state transition diagram of an instruction cycle.

   c) What is interrupt ? What is the difference between vectored & non-vectored interrupts ?

   d) Why is DMA mode of data transfer used ? What are the different types of DMA controllers and how do they differ in their functioning ?

   1 + (2 + 1 + 3) + (1 + 2) + (2 + 3)

10. a) Explain the difference between full associative and direct mapping techniques.

    b) What are the different types of ROM ? Explain their principles.

    c) How much 128 × 16 RAM chips are needed to construct a memory capacity of 4096 words (16 bit in one word) ? How many lines of the address bus must be used to access a memory of 4096 words ? 5 + 5 + 5

11. a) What is instruction cycle ? Describe addressing modes.

    b) Explain the basic DMA operations for transfer of data between memory and peripherals.

    c) Evaluate the arithmetic statement $X = (A * B)/(C + D)$ in one, two and three address machines. 1 + 4 + 5 + 5

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