ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2007

MICRO-PROCESSOR AND MICRO-CONTROLLER

SEMESTER – 5

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) The interrupts pin available in the 8085 *A* microprocessor chip is

a) ALE b) $\overline{\text{HLDA}}$

c) INTR d) SOD. ☐

ii) For 8255 PPI, the bidirectional mode of operation is supported in

a) Mode 1 b) Mode 2

c) Mode 0 d) either (a) or (b). ☐

iii) 8086 exchanges data word with odd memory bank when

a) $\overline{\text{BHE}} = 0$ and $A_0 = 0$ b) $\overline{\text{BHE}} = 0$ and $A_0 = 1$

c) $\overline{\text{BHE}} = 1$ and $A_0 = 0$ d) $\overline{\text{BHE}} = 1$ and $A_0 = 1$. ☐

iv) If ready pin is grounded, it will introduce ..... states into the bus cycle of 8086 / 8088 µp.

a) wait b) idle

c) wait and remain idle d) all of these. ☐

v) What are the conditions that BIU can suspend fetching instruction ?

a) Current instruction requires access to memory or I/O port

b) A transfer control (Jump or call) instruction occurs

c) Instruction queue is full

d) All of these. ☐

vi) RST 7·5 interrupt is

a) Vectored & Maskable b) Vectored and Non-Maskable

c) Direct & Maskable d) Direct & Non-Maskable. ☐

vii) In "JZ NEXT" instruction of 8051 microcontroller, which register's content is checked to see if it is zero ?

a) *A* b) *B*

c) *R* 1 d) *R* 2. ☐

viii) If a DMA request is sent to the microprocessor with a high signal to the HOLD pin, the microprocessor acknowledge the request

a) after completing the present cycle

b) immediately after receiving the signal

c) after completing the program

d) none of these. ☐

ix) When the RET instruction at the end of a sub-routine is executed

a) the information where the stack is initialized is transferred to the stack pointer

b) the memory address of the RET instruction is transferred to the PC

c) two data bytes stored in the top two locations of the stack are transferred to the PC

d) two data bytes stored in the top two locations of the stack are transferred to the SP. ☐

x) Whenever the POP H instruction is executed

a) data bytes in the HL pair are stored on the stack

b) two data bytes at the top of the stack are transferred to the HL register pair

c) two data bytes at the top of the stack are transferred to the PC

d) two data bytes from the HL register that were previously stored on the stack are trnsnferred back to the HL registers. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following questions. $3 \times 5 = 15$

2. What are the advantages of having segmentation ? How does the 8086 microprocessor support segmentation ?

3. If the system clock is 2 MHz, find the time to execute the given instruction code :

MVI A, $(5A)_H$

MVI B, $(A7)_H$

ADD B

INR A

XRA A

HLT / RST 1.

4. Find the memory address range for the following diagram shown below :

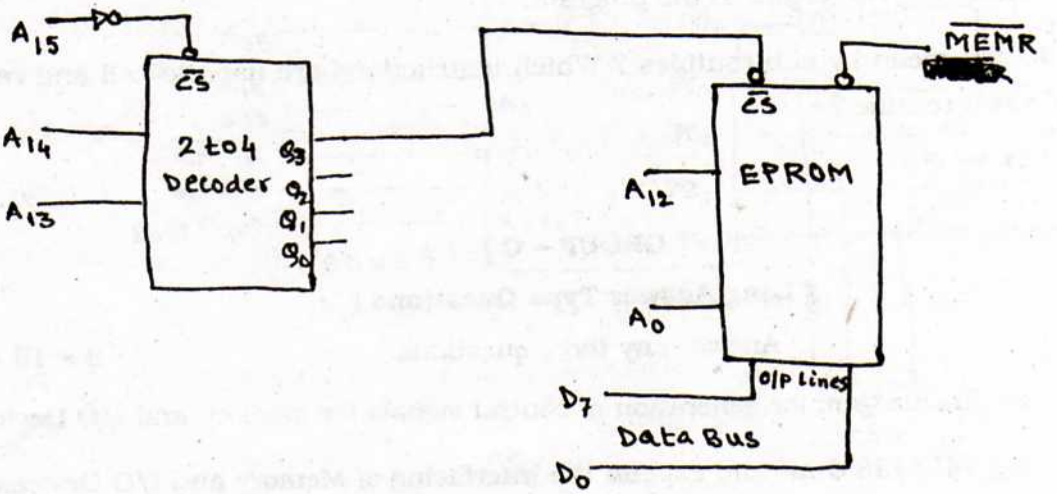

Fig. 1

5. The following program adds the number of bytes stored in memory locations starting from 2100 H and saves the result in memory. Read the program and answer the questions given below :

```
        LXI H, 2100H
        LXI D, 0000H
NEXT :  ADD M
        JNC SKIP
        INR E
SKIP :  DCR D
        JNZ NEXT
        LXI H, 2090H
        MOV M, A
        INX H
        MOV M,E
        HLT
```

a) Assuming the byte counter is set-up appropriately, specify the number of bytes that are added by the program. 2

b) Specify the memory locations where the result is stored. 2

c) Identify the two errors in the program. 1

6. What do you mean by sub-routines ? Which instructions are used to call and return from the sub-routine ? 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. 3 × 15 = 45

7. a) Draw the diagram for generation of control signals for memory and I/O Devices.

b) Using 74LS138 draw and explain the Interfacing of Memory and I/O Devices.

c) Draw the organization of a memory chip and also mention the lines used by the Memory chip to communicate with the MPU. 5 + 5 + 5

8. a) Describe the different addressing modes of 8086 microprocessor.

b) What are the main functions performed by BIU & EU unit of 8086 microprocessor ?

c) How is pipelining achieved in 8086 microprocessor ? 4 + (4 + 4) + 3

9. a) List the operating modes of the 8255A PPI. 2

b) Specify the bit of a control word for the 8255, which differentiates between the I/O mode and the BSR mode. 1

c) Write initialisation instruction for the 8255 *A* to set up port *B* as an O/P port in mode 0. 2

d) List the major sections of the 8279 programmable keyboard/Display interface. 2

e) Write a program to read the DIP switches and display the reading from port *B* (I/O port) at port *A* (O/P port) and from port *C* (I/O port) at port *C* (I/O port) for the fig. 2 shown below. 8

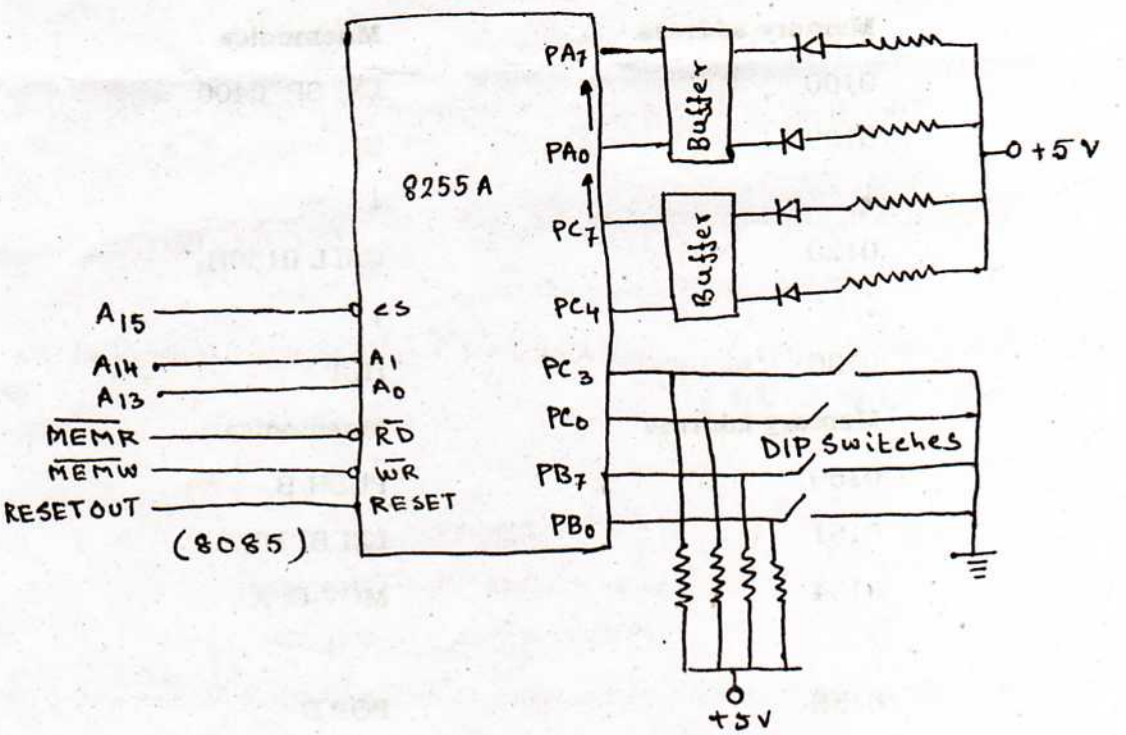

Fig. 2

10. a) A set of eight data bytes is stored in the memory location starting at XX50H. Check each data byte for bits D_7 and D_0. If D_7 or D_0 is 1, reject the data byte ; otherwise, store the data bytes at memory locations starting at XX60H.

b) Describe the different modes of operation of 8253 timer.

c) What do you mean by 16 bit microprocessor ?

d) Explain the function of RIM instruction.

e) What is the purpose of DMA controller ? 5 + 5 + 1 + 2 + 2

11. a) The main program is stored beginning at 0100 H. The main program (at 0120 H) has called the sub-routine at 0150 H, when the μp is executing the instruction at location 0151 H, it is interrupted. Read the following program, then answer the questions :

Memory address	**Mnemonics**
0100	LXI SP, 0400
0103	EI
↓	↓
0120	CALL 0150H
↓	↓
0130	HLT
Memory address	**Mnemonics**
0150	PUSH B
0151	LXI B, 10FF
0154	MOV C, A
↓	↓
015E	POP B
015F	RET

i) Assuming before CALL 0150H, the stack was not used, specify the content of top two locations of the stack.

ii) Specify the stack locations where the contents of register pair *B* are stored.

iii) When a program is interrupted, what is the memory address stored on the stack ?

b) Describe the priority scheme & EOI scheme of 8259.

c) Write down the format of ICW1 & ICW2 of 8259.

d) What do you mean by conditional and unconditional RET instruction in 8085 Microprocessor ? Explain with example. 3 + 5 + 4 + 3

END