



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (ICE/EEE/EE(O)/PWE)/SEM-4/EC-402/2011

2011

**DIGITAL ELECTRONICS AND INTEGRATED
CIRCUITS**

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

- i) In which code do the successive code characters differ in only one position ?

- a) Hamming code b) Excess-3 code
c) Gray code d) ASCII code.

- ii) If t_p is the pulse width, Δt is the propagation delay and T is the period of pulse train, then which one of the following conditions can avoid the race around conditions ?

- a) $t_p = \Delta t = T$ b) $2t_p > \Delta t > T$
c) $t_p < \Delta t < T$ d) $2t_p < \Delta t < T$.



iii) The equation $\sqrt{213} = 13$ is valid for which one of the number systems with base ?

- a) Base 8
- b) Base 6
- c) Base 5
- d) Base 4.

iv) The minimum number of flip-flops required to design a MOD-10 counter is

- a) 03
- b) 10
- c) 04
- d) 05.

v) The maximum number of function generated by 4 input variables is

- a) 16
- b) $2^4 - 1$
- c) 56636
- d) 65536.

vi) A bubbled AND gate is equivalent to a

- a) OR gate
- b) NAND gate
- c) NOR gate
- d) X-OR gate.

vii) A code used for labelling the cells of a K-map is

- a) 8-4-2-1 binary
- b) Hexadecimal
- c) Gray
- d) Octal.



viii) Which one of the following is a self complementing code ?

- a) Ex-3 code
- b) Gray code
- c) 8421 code
- d) None of these.

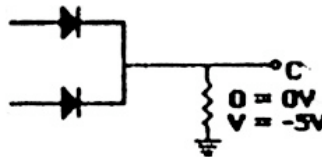
ix) A clock frequency of 100 kHz is applied to MOD – 8 followed by a decade counter. What will be the output frequency ?

- a) 12.5 kHz
- b) 10 kHz
- c) 1.25 kHz
- d) None of these.

x) A 3-bit synchronous counter uses flip-flops with propagation delay time of 20 ns each. The maximum possible time required for change of state will be

- a) 60 ns
- b) 40 ns
- c) 20 ns
- d) none of these.

xi) If the negative logic is used, the diode gate shown in the given figure will represent



- a) OR gate
- b) AND gate
- c) NOR gate
- d) NAND gate.



xii) The minimum number of NAND gates required to implement $A + A\bar{B} + A\bar{B}C$ is equal to

- a) 0
- b) 1
- c) 4
- d) 7.

xiii) The race-around condition does not occur in flip-flop.

- a) J-K
- b) Master slave
- c) T
- d) None of these.

xiv) $(11011)_2$ in BCD 8421 code is

- a) 00011011
- b) 00100111
- c) 11011001
- d) 01101100.

xv) For a shaft encoder, the most appropriate 2-bit code is

- a) 11,10,01,00
- b) 11,10,00,01
- c) 01,10,11,00
- d) 01,00,11,10.



GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following.

3 × 5 = 15

2. What is fan-out ? What is the basic difference between a latch and an edge triggered Flip-Flop ?
3. Design a full adder using 3 : 8 decoder with all active low outputs and additional logic gates if required.
4. Realize the following function by minimum number of 2-input NAND gates only
$$F (A, B, C, D) = B (A + CD) + AC$$
5. Draw the output waveform of J-K flip-flop for input sequence J = 1011010 and K = 0110110
 - a) The Flip-Flop is positive edge-triggered
 - b) The Flip-Flop is negative edge-triggered.
6. With the help of a block diagram, explain the working principle of a serial adder.

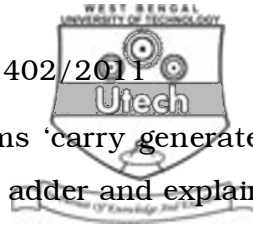
GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following.

3 × 15 = 45

7. a) Implement the following function using 3 × 4 × 2 PLA :
$$F_1(A, B, C) = \sum(3, 5, 6, 7), F_2(A, B, C) = \sum(0, 2, 4, 7).$$
 - b) Describe the R-2R ladder type D/A converter.
 - c) What do you mean by resolution ?

6 + 8 + 1



8. a) What is CLA adder ? Define the terms 'carry generate' and 'carry propagate'. Design the CLA adder and explain its operation.
- b) What are the differences between serial adder and parallel adder ?
- c) Design a logic diagram using logic gates and four full adder module for addition/subtraction, a control variable P such that this operate as full adder when $P = 0$ and full subtractor when $P = 1$.
- $$(1 + 2 + 5) + 2 + 5$$
9. a) Explain the operation of dual slope integration type A/D converter. Derive the expression of the output voltage.
- b) Draw the circuit diagram of 2 input TTL NAND gate and explain how it works. Write down the truth table.
- c) What do you mean by resolution ? $7 + 7 + 1$
10. a) What are the facilities available in universal shift register ? How can a 4-bit universal shift register be realized using multiplexers and Flip-Flops.
- b) Write down the count sequence of a 3-bit binary Down Counter. Design a Ripple counter using negative edge triggered T Flip-Flops for the sequence.
- c) What is race-around condition ? How it can be eliminated ? $7 + 5 + 3$



11. a) Simplify the Boolean function :

$$F = \sum_m (0, 2, 3, 6, 7) + \sum_d (8, 10, 11, 15)$$

Using K-map

method.

- b) Design a full subtractor circuit with the help of full-adder circuit and one NOT gate. Write down the expression & truth table in favour of your design.
- c) Which code is known as self complementing code ?

Explain your answer.

7 + 5 + 3
