CS/B.Tech (EE-New)/SEM-5/EE-504C/2013-14

2013

MICROPROCESSOR & MICROCONTROLLER

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) Whenever the PUSH instruction is executed in case of 8085 CPU, the stack pointer is

a) decremented by 1 b) decremented by 2

c) incremented by 1 d) incremented by 2.

ii) Address line required for 32k-byte memory chip is

a) 13 b) 14

c) 15 d) 16.

iii) How many hardware interrupt requests a single interrupt controller IC8259A can process ?

a) 8 b) 15

c) 16 d) 64.

iv) In DMA operation, data transfer takes place between

a) Memory & CPU b) CPU & I/O

c) I/O & Memory d) Different CPUs.

v) When the instruction LHLD is executed, the No. o *T*-states required is

a) 10 b) 14

c) 13 d) 15.

vi) How many flag registers are there in 8051 ?

a) 9 b) 8

c) 6 d) 5.

vii) The interrupt masks in 8085 can set or reset by the instruction

a) EI b) DI

c) RIM d) SIM.

viii) The vector address corresponding to software interrupt command RST7 in 8085 microprocessor is

a) 0017 H b) 0027 H

c) 0038 H d) 0700 H

ix) The instruction that does not clear accumulator content is

a) XRA A b) ANI FFH

c) MVI A, 00H d) None of these.

x) MVI B, 89H; MOV A, B; XRA A; OUT PORT; HLT

After the execution of program the output of PORT is

a) 89 H b) 37 H

c) 07 H d) 00 H.

xi) 8085 μP has connected with a crystal of 2 MHz. operating frequency is

a) 4 MHz b) 1 MHz

c) 2 MHz d) 3 MHz.

xii) For MVI A, 05 H

the number of *T*-states required is

a) 4 b) 3

c) 7 d) 10.

xiii) The number of bytes in the instruction RST 3 is

a) 2 b) 3

c) 1 d) 4.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain the need to de-multiplex the bust AD0-AD7. Show how it can be demultiplexed in 8085 microprocessor. 2 + 3

3. a) What are the functions ALE, HOLD and READY ?

b) Discuss the function of following instruction of 8085 :

LHLD C020, DCXB. 2 + 3

4. What are interrupts ? How many interrupts are there in 8085 ? What are the maskable and non-maskable interrupts ? Discuss SIM instruction. 2 + 2 + 1

5. Interface 2K × 8 RAM with 8085 microprocessor by using IC 74138 such that starting address assign to them are 8000 H.

6. a) Define instruction cycle and machine cycle.

b) Specify the register contents and the flag status as the following instructions are executed. Specify also the data at Port 76H. Initial contents of

A = 00H, B = FFH, S = 0, Z = 1, CY = 0

MVI A F2H

MVI B 7AH

ADD B

OUT 76H

HLT

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) How many ports are there in 8255 and what are they ?

   b) Discuss the different bits of the control word of 8255.

   c) Write down the MODE-0 control word for the following :

      i) Port A = Input

      ii) Port B not used

      iii) Port C upper = Input, Port C lower = output

   d) Discuss BSR operation of 8255. 2 + 5 + 3 + 5

8. a) Explain how 20-bit physical address is generated in 8086 microprocessor.

   b) What is the purpose of queue ? How many words does the queue store in 8086 microprocessor ?

   c) How does 8086 support pipelining ? Explain.

   d) What are the advantages of having memory segmentation ? 3 + 1 + 3 + 5 + 3

9. a) The following block of data is stored in the memory locations from XX55(H) to XX5A(H). Transfer the data to the locations XX80(H) to XX85(H) in the reverse order. [e.g. the data byte 22H should be stored at XX85(H) and 37H at XX80(H)]. Data(H) : 11, B5, C2, 95, 7F & 39.

   b) Write the control word format for I/O mode in 8255.

   c) Write a program to set PC_4 & reset PC_7 times using BSR mode in 8255. 5 + 5 + 5

10. a) What do you mean by subroutine ? Briefly discuss the sequence of events that take place while executing CALL instruction.

    b) Briefly describe the DMA operation. Which IC is used for this purpose ?

    c) What are the differences between a microprocessor and a microcontroller ? Discuss the memory organization of 8051 microcontroller. 5 + 5 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Conditional return instructions of 8085

b) DMA controller

c) Subroutine

d) Stack memory

e) Operating mode of 8255.