



Name :

Roll No. :

Invigilator's Signature :

**CS/B.Tech(EE-OLD)/SEM-4/EC(EE)-402/2012
2012**

DIGITAL ELECTRONICS & INTEGRATED CIRCUITS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

i) Identify the carry expression of full adder circuit

- a) $X'Y + ZX'$
- b) $XY + YZ + ZX$
- c) $XY' + YZ' + ZX$
- d) $X'Y' + XZ' + YZ$

ii) Which one is used in EPROM eraser ?

- a) Laser light
- b) UV ray
- c) LED light
- d) Sunrays.



iii) Gray code of 1011 (binary) =

- a) 0101 b) 1101
- c) 1110 d) none of these.

iv) What is the next octal counting sequence 724, 725, 726, 727 ?

- a) 728 b) 729
- c) 730 d) 731.

v) The equation $\sqrt{(213)} = 13$ is valid for which one of the number system with base ?

- a) Base 8 b) Base 6
- c) Base 5 d) Base 4.

vi) A 10 MHz signal is applied to a MOD-5 counter followed by a MOD-8 counter then the o/p frequency will be

- a) 10 kHz b) 2.5 kHz
- c) 5 kHz d) 250 kHz.



vii) Calculator keyboard is an example of

- a) decoder
- b) encoder
- c) multiplexer
- d) demultiplexer.

viii) A single bit memory device is

- a) ROM
- b) RAM
- c) F-F
- d) PROM.

ix) The octal equivalent of the binary number 11010111 is

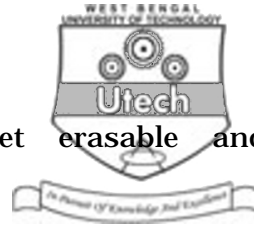
- a) 656
- b) 327
- c) 653
- d) D7.

x) The minimum number of NAND gates required to implement the Boolean function $A + AB' + AB'C$ is equal to

- a) zero
- b) 1
- c) 4
- d) 7.

xi) The fastest logic gate family is

- a) CMOS
- b) ECL
- c) TTL
- d) RTL.



xii) The memory, which is ultraviolet erasable and electrically programmable is

- a) RAM
- b) EEROM
- c) EPROM
- d) PROM.

xiii) A ring counter consists of 5 flip-flops will have

- a) 5 states
- b) 10 states
- c) 32 states
- d) none of these.

xiv) The flip-flop, which is free from race around problem is

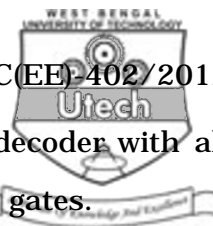
- a) R-S flip-flop
- b) Master-slave JK flip-flop
- c) J-K flip-flop
- d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Explain the race around condition. Draw the Master/Slave JK flip-flop using all NAND gates. $2 + 3$



3. Implement a full-adder circuit using 3 to 8 decoder with all active high outputs and other necessary logic gates.
4. Draw and explain the circuit of 8×1 MUX using two 4×1 MUX and one 2×1 MUX.
5. Minimize the following expression in SOP form using Quine McClusky method :

$$F(A, B, C, D) = \sum m(1, 2, 3, 8, 9, 10, 11, 14) + \sum d(7, 15).$$

6. Perform the arithmetic operation :

$$(-22)_{\text{decimal}} + (13)_{\text{decimal}} + (-15)_{\text{decimal}}$$

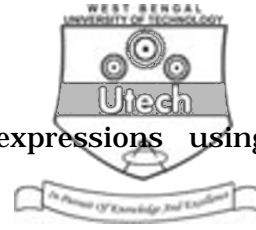
using 2's complement binary form.

GROUP - C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. Write short notes on any *three* of the following : 3×5
 - a) EPROM
 - b) A/D converter
 - c) Parity generator
 - d) Tri-state gates in TTL family
 - e) Data Lock-out in a counter.



8. a) Implement the following Boolean expressions using Decoder.

$$F_1 (A, B, C, D) = \sum (1, 2, 5, 7, 8, 10, 12, 13). \quad 5$$

- b) Implement a full adder circuit using minimum number of NOR gates only. 5

- c) An 8 : 1 MUX has inputs A, B, C connected to select line S_2, S_1, S_0 respectively. The data inputs I_0 to I_7 are connected as $I_1 = I_2 = I_7 = 0$,

$$I_3 = I_5 = 1, \quad I_0 = I_4 = D, \quad I_6 = D'. \quad \text{Determine the Boolean expression of the MUX output.} \quad 5$$

9. a) Design MOD-10 synchronous UP-counter using the JK flip-flops and other required logic gates. 10

- b) Calculate the propagation delay for a 4-bit synchronous UP-counter when JK flip-flops are connected in series connection and parallel connection. Given propagation delay $t_p (FF)$ equals to 30 nsec and the propagation delay of the gates used in the circuit are 20 nsec (assumed to be equal for all gates). 5

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10. a) Construct a 4-bit register with parallel load. 10
- b) Describe the basic principles of Successive Approximation Method for A/D converter. 5

