EC(EE)-302

DIGITAL ELECTRONIC CIRCUITS

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) The fastest logic family is

(A) TTL (B) CMOS
(C) RTL (D) ECL

(ii) A flip-flop has

(A) one stable state (B) two stable states
(C) three stable states (D) none of these

(iii) A decoder with enable input can be used as

(A) encoder (B) parity generator
(C) multiplexer (D) de-multiplexer

(iv) The minimum no. of NAND gates required to design one full adder circuit is

(A) 5 (B) 9
(C) 6 (D) 10

(v) Which family has better noise margin?

(A) TTL (B) ECL
(C) DTL (D) MOS

(vi) Master slave configuration is used in flip flop to

(A) increase its clocking rate (B) reduce power dissipation
(C) eliminate race around condition (D) improve its reliability

(vii) The power consumption of a dynamic RAM is

(A) equal to static RAM (B) more than static RAM
(C) less than static RAM (D) almost zero

(viii) How many full adders are required to construct m bit parallel adder?

(A) m/2 (B) m
(C) m – 1 (D) m + 1

(ix) An example of self-complementing code is

(A) BCD (B) GRAY
(C) ASCII (D) Excess-3

(x) The simplified form of the Boolean expression (X + Y' + Z) (X + Y' + Z') (X + Y + Z) is

(A) X'Y + Z (B) X + Y'Z
(C) X'Y + Z' (D) XY + Z'

(xi) The code used for labeling cell of the K-map is

(A) natural BCD (B) hexadecimal
(C) gray (D) octal

(xii) A modulus 10 Johnson counter requires

(A) ten flip-flops (B) four flip-flops
(C) five flip-flops (D) twelve flip-flops

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Implement the following expression using NOR gate only 5
$F(A, B, C) = \sum m(0, 1, 4, 6)$

3. (a) Can a decoder be used as a demultiplexer? If it is possible what hardware feature should be present with the decoder? 2+3

(b) Cascade two 2-to-4 decoders to form 3-to-8 decoder.

4. Implement a full adder circuit using 3 to 8 decoder with all active high outputs and other necessary logic gates. 5

5. Explain parallel in serial out shift register with block diagram. 5

6. (a) Differentiate combinational logic circuit and sequential logic circuit. 2+3

(b) Minimize the following function using K-map
$F(A,B,C,D) = \Sigma_m(0,2,3,6,7) + \Sigma_d(8,10,11,15)$ and implement the circuit using basic gates.

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) Draw and explain the BCD adder circuit using commercially available IC-7483 and other necessary logic gates. 7

(b) Design a combinational circuit using ROM that accepts 3-bit number and generate the output binary number equal to square of input number. 5

(c) Design Binary to gray code converter using logic gates. 3

8. (a) Write the truth-table, circuit diagram, waveform and state diagram of J-K flip-flop. 8+7

(b) Convert D flip-flop to J-K flip-flop.

9. (a) What are the differences between LATCH and flip-flop?

(b) Design MOD-3 synchronous counter using J-K flip-flop.

(c) Design MOD-6 ripple counter using negative edge trigger J-K flip-flop.

10.(a) Explain the operation of R-2R Ladder type DAC with neat circuit diagram.

(b) Explain the working of a successive approximation register (SAR) type ADC.

11. Write short notes on any *three* of the following:

(a) 2-bit comparator

(b) Odd parity generator and checker

(c) Parallel in serial out (PISO) shift register

(d) Tri-state gates in TTL family

(e) Johnson counter