CS/B.Tech/EE/EEE/ICE/Odd/Sem-3rd/EC(EE)-302/2015-16

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

EC(EE)-302

DIGITAL ELECTRONIC CIRCUIT

Time Allotted: 3 Hours   Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. $10 \times 1 = 10$

   (i) The number of bit required to represent an eight digit decimal number in BCD is

   (A) 8   (B) 16
   (C) 24   (D) 32

   (ii) All Boolean expression can be implemented with

   (A) NAND gate only   (B) NOR gate only
   (C) Combination of all basic gates   (D) Any of these

   (iii) The minimum number of NAND gates required to implement the Boolean function $A + \bar{A}B + A\bar{B}C$ is

   (A) three   (B) two
   (C) one   (D) zero

3105   1   Turn Over

   (iv) Which of the following flip-flop is used as a latch?

   (A) J-K flip-flop   (B) S-R flip-flop
   (C) D flip-flop   (D) T flip-flop

   (v) A full adder can be made out of

   (A) two half adder   (B) two half adder and an inverter
   (C) two half adder and a OR gate   (D) two half adder and a AND gate

   (vi) An asynchronous counter is also known as

   (A) ripple counter   (B) multiple clock counter
   (C) decade counter   (D) modulus counter

   (vii) A MOD 13 counter must have

   (A) 13 flip-flop   (B) 3 flip-flop
   (C) 4 flip-flop   (D) 2 flip-flop

   (viii) Which of the following is an invalid state of an 8241 BCD counter?

   (A) 0010   (B) 0101
   (C) 1000   (D) 1100

   (ix) The fan out of a logic gate refers to number of

   (A) input device that can be connected
   (B) input terminal
   (C) output terminal
   (D) circuit that can be connected at the output

   (x) Static RAM is preferred over dynamic RAM when the requirement is of

   (A) slow speed of operation   (B) large storage capacity
   (C) lower access time   (D) lower power consumption

   (xi) A PLA can be used

   (A) as a microprocessor   (B) as a dynamic memory
   (C) to realize a sequential circuit   (D) to realize a combinational circuit

3105   2

CS/B.Tech/EE/EEE/ICE/Odd/Sem-3rd/EC(EE)-302/2015-16

(c) Design a full subtractor using two half-subtractors and one extra gate, if necessary.

9. (a) Describe the operation of successive approximation type ADC.

(b) Explain the sequence of operation of conversion of an analogue signal to its digital equivalent when the expected digital output is 1010.

(c) Define quantizing error for an ADC.

10.(a) What is the significance of the logic family with reference to digital Integrated Circuits (ICs)?

(b) What is the totem-pole output stage? What are its advantages?

(c) Implement the following functions using PROM:

$$F1(A,B,C) = \sum m(0, 2)$$
and
$$F2(A,B,C) = \sum m(1, 4, 7)$$

11. Write short notes on any *three* of the following:

(a) Lock-out phenomena in counters

(b) Irregular counter

(c) PAL

(d) Encoder

(e) CMOS and its operation

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. $3 \times 5 = 15$

2. Obtain the logic expression for a 3-input majority function and hence implement it using only NAND gates.

3. Design 4:1 multiplexer using 2:1 multiplexer.

4. Prove that $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$.

5. Using 2's complement method subtract $(101101)_2$ from $(1011101)_2$.

6. Convert J-K flip-flop to D flip-flop.

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. (a) Simplify the following function using K-map: 7

$$f = \sum m(0, 5, 8, 10, 11, 14, 15) + \sum d(3, 13).$$

(b) What are the difference between minterms and maxterms?   2

(c) Prove Distributive law and Absorption law.   6

8. (a) What is the difference between full-adder and full-subtractor?   4

(b) Show how a full-adder can be converted to a full-subtractor with the addition of an inverter circuit.   5