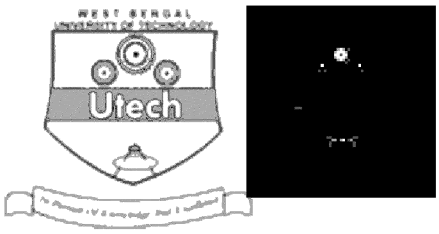
EDA FOR VLSI DESIGN (SEMESTER - 7)

CS/B.TECH (ECE)/RE/SEM-7/EC-702/09



1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

CS/B.TECH (ECE)/RE/SEM-7/EC-702/09

ENGINEERING & MANAGEMENT EXAMINATIONS, APRIL – 2009

EDA FOR VLSI DESIGN (SEMESTER - 7)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **marked 'Answer Sheet'**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

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FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B			Group – C				
Question Number																	***Total Marks***	***Examiner's Signature***
Marks Obtained																		

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Head-Examiner/Co-Ordinator/Scrutineer

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GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Which one of the following statement is *False* ?

a) Multiplexer can be used as a programmable logic device

b) An EPROM can be used as a programmable logic device

c) A Flip-flop can be made using OR gate and AND gate only

d) A Microprocessor based system can be used for implementing complex logic function.

ii) VHDL is a

a) sequential language b) concurrent language

c) test language d) all of these.

iii) Which one of the following is *True* ?

a) Microprogram control unit is faster than hardwired logic control unit

b) FPGAs are faster than ASIC

c) LUTs can be implemented using EPROM

d) None of these.

iv) PLA (Programmable Logic Array) has

a) fixed OR plane followed by programmable AND plane

b) programmable AND plane followed by fixed OR plane

c) fixed AND plane followed by programmable OR plane

d) programmable AND plane followed by programmable OR plane.

v) Which of the following statements is *False* ?

a) PROM uses fusible link

b) There is restriction on the inputs and outputs in a PLA

c) A PLA is faster than PAL

d) Both (a) & (b).

vi) Which of the following is an ASIC ?

a) A DSP processor b) An FPGA

c) FFT processor d) Both (a) & (b).

vii) VLSI design flow is a

a) cyclic process only b) parallel process

c) sequential and cyclic process d) none of these.

viii) Output of physical design is

a) circuit b) layout

c) logical model d) RTL schematic.

ix) Which stages in electronic system design process can VHDL be applied to ?

a) only ASIC, FPGA or CPLD design

b) only specifying the hardware part of the system

c) only specifying the system before it is partitioned into hardware and software

d) all stages mentioned in choices a, b & c.

x) The logic family which consumes least amount of power is

a) DTL b) RCTL

c) CMOS d) none of these.

xi) LUT is used in

a) CPLD b) PLD

c) FPGA d) none of these.

xii) The fastest logic family is

a) TTL b) CMOS

c) ECL d) RTL.

xiii) Programmable System On Chip (PSOC) is

a) more flexible compared to FPGA

b) more flexible compared to ASIC

c) faster than ASIC

d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) What is layout ? 2

b) Draw the layout of CMOS, NAND gate. 3

3. a) Write VHDL code in RTL level to implement a F/F (Flip-flop). 3

b) What do you mean by 'FOX' in IC fabrication ? 2

4. a) What restrictions are placed on VHDL that is to be written for today's synthesis tool ? Explain your justification. 3

b) VHDL is a language that allows the user to describe the activities that are happening in parallel. Explain with an example statement. 2

5. a) A VHDL description can also sequential. Explain with example. 2

b) What are the different levels of abstraction in VHDL ? 2

c) What do you mean by 'components' in VHDL ? 1

6. Draw the physical mask layout for $2 \times 2\frac{1}{2}$

a) a half adder

b) NOT gate.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) Draw the block diagram an FPGA and explain the operation in detail. 8

   b) Explain with block diagram, the configuration process of FPGA. 7

8. a) What do you mean by FPGA design cycle ? Explain each steps in the design cycle. 8

   b) Write a VHDL code to design a four bit register for loading input data. A control signal 'LOAD' is employed such that when LOAD signal is high, data will be stored. The operation is however synchronized with the rising edge of the clock. 7

9. a) Using a 8 × 1 MUX, how a three variable logic function can be designed ?

   b) Write a VHDL code for such an MUX.

   c) Convert the MUX to a 8 × 1 bit non-volatile memory. 5 + 5 + 5

10. a) What do you mean by 'Stuck-at-1" fault and "Stuck-at-0" fault ? Give a logic example. 5

    b) What is JTAG ? What is boundary scan ? 4

    c) Explain the terms "Simulation" & "Synthesis" in the context of FPGA. 4

    d) What is cell library ? 2

11. Write short notes on any *three* of the following : 3 × 5

    a) Placement, floor planning and routing

    b) Timing analysis, verification and validation

    c) Test generation

    d) Analog design automation tools

    e) *n*-well CMOS fabrication process.

END