



Name :

Roll No. :

Invigilator's Signature :

CS/B.Tech (ECE-NEW)/SEM-6/EC-604/2010
2010
VLSI CIRCUITS AND SYSTEMS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

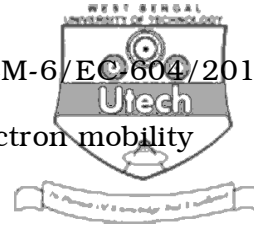
*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

- i) Scaling is done for
 - a) improving the switching speed
 - b) reducing the power dissipation
 - c) decreasing the chip size
 - d) all of these.
- ii) For $0.25 \mu\text{m}$ process what is the value of λ ?
 - a) $0.5 \mu\text{m}$ b) $0.125 \mu\text{m}$
 - c) $0.75 \mu\text{m}$ d) $1 \mu\text{m}$.

- 2

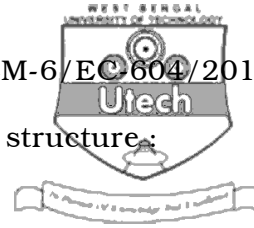


- ix) In a short channel MOS structure electron mobility
- a) increases
 - b) decreases
 - c) remains same
 - d) first increases then decreases.
- x) CMOS inverter is useful because it has
- a) low sensitivity to noise
 - b) low power consumption
 - c) excellent speed
 - d) all of these.
- xi) The main advantage of precharge-evaluate dynamic logic is
- a) lesser number of transistors required
 - b) high speed
 - c) low power consumption
 - d) all of these.
- xii) When two n MOS are connected in parallel, the equivalent k_n is given by
- a) $2k_n$
 - b) $k_n/2$
 - c) k_n
 - d) none of these.

- GROUP – B**

Answer any *three* of the following. $3 \times 5 = 15$

- 4



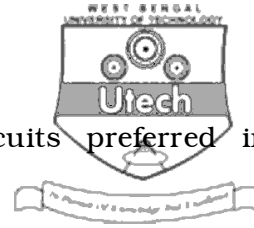
4. Describe the following phenomena in MOS structure:
 - a) I-V characteristics
 - b) Channel length modulation.
5. a) What do you mean by CMOS Transmission Gate (TG).
 b) Design the following circuits using transmission gates : 2 + 3
 - i) 2 input XOR gate
 - ii) 2×1 MUX.
6. Explain with a circuit diagram, operation of a differential amplifier.

GROUP – C

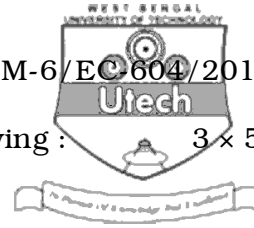
(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Design a transmission gate full adder circuit and explain.
 b) What are the differences between PLA and PAL ?
 c) Implement the following two functions using PLA and PAL.
 - i) $F1 = BA + C'B'A + CB'A'$
 - ii) $F2 = C'B'A' + CBA$. 5 + 5 + 5



8. a) Where are the dynamic logic circuits preferred in comparison to static logic ?
- b) What is domino CMOS logic ? How the cascading problem in dynamic logic can be eliminated in domino logic ?
- c) What is the charge sharing problem in dynamic CMOS logic ? How can it be prevented ?
- d) Describe the operation of three transistor DRAM cell.
- 2 + 4 + 4 + 5
9. a) What are the differences in between diffusion and ion implantation ?
- b) Explain the fabrication steps of CMOS inverter with necessary diagrams.
- 3 + 12
10. a) Show that for a symmetric CMOS inverter the two noise margins are same and are equal to V_{IL} . Also show that for ideal CMOS inverter $(W/L)_p = 2.5(W/L)_n$.
- b) What do you mean by design rules ? What are the differences in between lambda (λ) and micron (μ) rules.
- 10 + 5



11. Write short notes on any *three* of the following : 3 × 5

- a) Constant voltage scaling
- b) CMOS NORA logic
- c) Drain Induced Barrier Lowering (DIBL)
- d) CPLD
- e) Dynamic RAM.

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