	Utech
Name:	
Roll No.:	In Summer (V. Samueledge Stad Conference
Invigilator's Signature :	

CS/B.TECH/ECE(O)/SEM-5/EI(EC)-502/2012-13

2012

MICROPROCESSOR & MICROCONTROLLER

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

(Multiple Choice Type Questions)

1.	Choose the con	rect alternative	es for any te	en of the for	lowing:
				1	$0 \times 1 = 10$

- i) The control signal used to distinguish between I/O operation and memory operation is
 - a) ALE

b) IO/\overline{M}

c) SID

- d) SOD.
- ii) The control signal, HOLD is sent by 8085 in order to
 - a) inform I/O device that the address is being sent over the AD line
 - b) achieve separation of address from data
 - c) synchronize with low speed peripheral
 - d) to activate DMA.
- iii) The number of bytes of RAM contained in 8155 is
 - a) 256

b) 512

c) 1024

d) 2K.

5005(O) Turn over

CS/B.TECH/ECE(O)/SEM-5/EI(EC)-502/2012-13



iv)	In 'JZ next' instr	ruction of 8051 micro	controller in which
	register's conten	t is checked to see if:	it is zero?
	\	1) D	- O'Establish In Co.

a) A

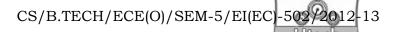
b) B

c) R1

- d) R2.
- If ready pin is grounded, it will introduce v) states into the BUS Cycle 8086/8088 microprocessors.
 - a) wait

- b) idle
- c) wait and remains idle d) all of these.
- vi) Whenever the POP H instruction is executed
 - a) data bytes in the HL pair are stored on the stack
 - b) two data bytes at the top of the stack are transferred to the HL reg. pair
 - c) two data bytes at the top of stack are transferred to the PC
 - d) two data bytes from HL reg. pair that were previously stored on the stack are transferred back to the HL registers.
- vii) For 8255 PPI, the bidirectional mode of operation is supported in
 - a) mode 1
- b) mode 2

- c) mode 0
- d) either (a) or (b).
- viii) If a DMA request is sent to the microprocessor with a HI signal to the HOLD pin, the microprocessor acknowledge the request
 - a) after completing the present cycle
 - b) immediately after receiving the signal
 - c) after completing the program
 - d) none of these.



- ix) STA 9000H is a
 - a) data transfer instruction
 - b) logical instruction
 - c) I/O and machine control instruction
 - d) none of these.
- x) The segment and offset address of the instruction to be executed by 8086 microprocessor are pointed by
 - a) CS and SI
- b) DS and IP
- c) CS and SP
- d) CS and IP.
- xi) The instruction register holds
 - a) flag conditions
- b) instruction address
- c) opcodes
- d) none of these.

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following

 $3 \times 5 = 15$

- 2. Explain the ALE IO/M signals of the 8085 microprocessor. Explain the need to demultiplex the bus $AD_7 AD_0$.
- 3. What are interrupts? How many interrupts are there? What are maskable & non-maskable interrupts? Discuss SIM instruction.
- 4. a) Write a ALP for a delay of 10 ms. Assume 3MHz to be the microprocessor clock frequency.
 - b) What are stack & subroutine?

3 + 2

- 5. What are the addressing mode available in 8085? Explain the instruction LDA & STA.
- 6. What are the advantages of segmentation ? How does the 8086 microprocessor support segmentation ?

CS/B.TECH/ECE(O)/SEM-5/EI(EC)-502/2012-13



(Long Answer Type Questions)

Answer any three of the following.

 $3 \times 15 = 45$

- 7. a) Draw the architecture of 8085 & mention its various functional blocks.
 - b) Discuss the function of the following signals of 8085: INTA, HOLD, READY, SID, SOD. 10 + 5
- 8. a) Divide 76_H by 04_H , the data are stored in 8100_H and 8101_H memory locations respectively.
 - b) Draw & explain the timing diagram for CALL instruction.
 - c) Discuss instruction cycle, machine cycle and *T*-state.

7 + 5 + 3

- 9. a) Write an ALP to find the sum of a series of 8 bit numbers, sum may be of 16 bits.
 - b) Explain the sequence of events that takes place when the PUSH & POP instructions are executed. Illustrate the operation of stack instructions with suitable examples.
 - c) Explain memory mapped I/O addressing and I/O mapped I/O addressing in 8085 microprocessor.

5 + 5 + 5

- 10. a) In how many modes can 8255 operate? Explain them.
 - b) Show the control word format for I/O mode operation of PPI 8255.
 - c) In mode 1, what are the control signals when port A &port B act as output ports. Discuss the control signals.
 - d) Discuss the mode 1 & mode 2 in which 8254 can operate. 5+3+3+4

=========