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CS / B.TECH (ECE-NEW) / SEM-5 / EC-503 / 2010-11

2010-11

COMPUTER ARCHITECTURE AND ORGANIZATION

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) The logic circuit in ALU is

a) entirely combinational

b) entirely sequential

c) combinational cum sequential

d) none of these.

ii) In a microprocessor the address of the next instruction to be executed is stored in

a) stack pointer

b) address latch

c) program counter register

d) general purpose.

iii) Physical memory broken down into groups of equal size is called

a) page b) tag

c) block d) index.

iv) The basic principle of a Von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) starting both program and data in the same memory

d) using a large number of registers.

v) The principle of locality justifies the use of

a) interrupts b) DMA

c) polling d) cache memory.

vi) Instruction cycle is

a) fetch-decode-execution

b) fetch-execution decode

c) decode-fetch-execution

d) none of these.

vii) Associative memory is a

a) pointer addressable memory

b) very cheap memory

c) content addressable memory

d) slow memory.

viii) Conversion of $(FAFAFA)_{16}$ into octal form is

a) 76767676 b) 76575372

c) 76737672 d) 76727672.

ix) The technique of placing software in a ROM semiconductor chip is called

a) PROM b) EPROM

c) Firmware d) Microprocessor.

x) How many address bits required for a 512 × 4 memory ?

a) 512 b) 4

c) 9 d) A0-A6.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain the reading & writing operations of a basic static MOS cell.

3. Give the Booth's algorithm for multiplication of signed 2's complement number in flowchart and explain.

4. Explain the concept of virtual memory.

5. What is Von Neumann architecture ? What is Von Neumann bottleneck ?

6. a) What are the widths of data bus and address bus for 4096 × 8 memory ?

   b) What do you mean by program status word ? 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Compare parallel adder with serial adder.

   b) Briefly describe Carry-Look-Ahead adder.

   c) Multiply –5 by –3 using Booth's algorithm.

4 + 6 + 5

8. a) What is pipelining ?

   b) What are speedup, throughput and efficiency of a pipelined architecture ?

   c) Describe pipeline hazards.

   d) What do you mean by paging ?

   e) What are instruction pipeline and arithmetic pipeline ? 2 + 3 + 5 + 2 + 3

9. a) Explain the basic Direct Memory Access (DMA) operation for transfer of data bytes between memory and peripherals.

b) Give the main reason why DMA based I/O is better in some circumstances than interrupt driven I/O.

c) What is programmed I/O technique ? Why is it not very useful ?

d) According to the following information, determine size of the subfields (in bits) in the address for Direct Mapping and Set Associative Mapping cache schemes:

- We have 256 MB main memory and 1 MB cache memory
- The address space of the processer is 256 MB
- The block size is 128 bytes
- There are 8 blocks in a cache set. 5 + 3 + 3 + 4

10. a) Evaluate the following arithmetic expression using 0, 1, 2, 3 address instruction :

$X = (A + B)/(C * D)$.

b) Why do we require memory hierarchy ? Show the memory hierarchy diagram indicating speed and cost.

c) Distinguish between SRAM and DRAM.

8 + (2 + 2) + 3

11. Write short notes on any *three* of the following : 3 × 5

a) Bus organization using Tri-state Buffer

b) Catch replacement policies

c) Restoring Division method

d) Comparison between RISC and CISC

e) Instruction format.

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