Nama :				Utech				
Invigilator's Signature :								
CS/B.TECH (ECE-OLD)/SEM-4/EC-402/2012								
2012								
DIGITAL ELECTRONICS CIRCUITS								
Time Allotted: 3 Hours				Full Marks : 70				
The figures in the margin indicate full marks.								
Candidates are required to give their answers in their own words								
as far as practicable.								
GROUP – A								
( Multiple Choice Type Questions )								
1. Choose the correct alternatives for any <i>ten</i> of the following :								
				$10 \times 1 = 10$				
i)	Decimal number + 52 and - 52 are							
	a)	0110100 & 1110100	b)	0101011 & 1101011				
	c)	0110100 & 1101011	d)	none of these.				
ii)	Addition of two hexadecimal numbers 58 and 24 is							
	a)	7E	b)	7C				
	c)	6B	d)	F1.				
iii)	2's c	s complement of hexadecimal number 73A is						
	a)	9C5	b)	8C6				
	c)	8B7	d)	8F1.				
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iv)	Nori	mally in HA circuit	which	gate is used for sum			
	part	?		A famo (y Excelege 2nd Excellent)			
	a)	XOR	b)	NAND			
	c)	OR	d)	AND.			
v)	Which one is the invalid code in Excess-3 code?						
	a)	0001 & 0000	b)	0110 & 0100			
	c)	1010 & 1100	d)	None of these.			
vi)	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a high output?						
	a)	1	b)	2			
	c)	7	d)	8.			
vii)	Which one of the following is reflected code?						
	a)	8421	b)	Gray			
	c)	Excess-3	d)	ASCII.			
viii)	If (212) $_x$ = (23) $_{10}$ then what is the value of $x$ ?						
	a)	2	b)	3			
	c)	4	d)	5.			
ix)	Which of the following codes is used in <i>K</i> -map for representing the minterm?						
	a)	BCD	b)	Gray			
	c)	8421	d)	Excess-3.			
x)	The example of a Moore machine is						
	a)	Sequence detector	b)	Binary counter			
	c)	BCD counter	d)	UP/DOWN counter.			
xi)	by a MOD-8 counter. The output frequency will be						
	a)	10 kHz	b)	2·5 kHz			
	c)	5 kHz	d)	25 kHz.			
xii)	A number of address lines in EPROM 4096 x 8 is						

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a)

c)

2

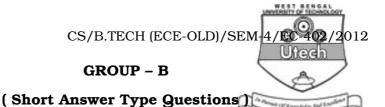
8

b)

d)

4

12.



Answer any three of the following.

 $3 \times 5 = 15$ 

- 2. Design a 2 bit comparator using logic gates.
- 3. Design a BCD adder circuit to add two BCD numbers maximum. The output of the adder should also be in BCD.
- 4. Minimize the following expressions using K map :  $F(A, B, C, D) = \pi M(0, 7, 8, 9, 10, 11, 15) + \phi(1, 4)$
- 5. Implement the function using only one 8: 1 max. Connect BCD with selection line.

$$F(A, B, C, D) = \sum m(0, 1, 2, 5, 9, 11, 13, 15)$$

6. What is 'race around problem'? How can it be overcome in JK flip-flop?

## **GROUP - C**

## (Long Answer Type Questions)

Answer any *three* of the following.  $3 \times 15 = 45$ 

- 7. a) Simplify the following functions by means of K-map :
  - i)  $F = \sum_{m} (0, 2, 6, 10, 11, 12, 13) + \sum_{d} (3, 5, 14).$
  - ii)  $F = \prod_{M} (0, 2, 6, 10, 11, 12, 13). \sum_{d} (6, 8, 10, 14).$
  - b) Design a common adder-subtractor and explain its function. 5 + 5 + 5
- 8. a) Write down the present state-next state table of JK & D flip-flops and derive the characteristic equation for these two flip-flops.
  - b) Draw logic diagram of the master-slave flip-flop. Why is it called so?
  - c) What are the differences between edge triggered and level triggered flip-flop. (3+3)+5+4

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- 9. a) Describe the operation of successive approximation type ADC. How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC?
  - b) Draw a neat diagram for an R-2R ladder type DAC and explain its operation. 7 + 8
- 10. a) Draw the circuit for a 4-bit Johnson counter using *D* flip-flop and explain its operation. Draw its timing diagram. How does its timing diagram differ from that of Ring counter?
  - b) Design a MOD-6 synchronous up-counter using JK flipflop. 8 + 7
- 11. Write short notes on any *three* of the following:

 $3 \times 5$ 

- a) EEPROM
- b) CMOS logic
- c) PLD
- d) Even parity generator & checker
- e) Comparator.

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