ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER – 2008

DIGITAL ELECTRONICS AND LOGIC DESIGN

SEMESTER - 3

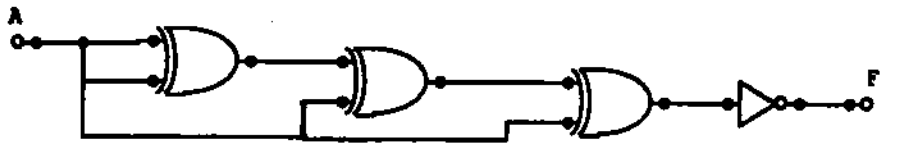
Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i)



The value of *F* is

a) 0 b) 1

c) A d) A'.

ii) The number of *XOR* gates required for the conversation of 11011 to its equivalent Gray Code is

a) 2 b) 3

c) 5 d) 4.

iii) The operation which is commutative but not associative is

a) AND b) XOR

c) NAND d) NOT.

8. a) Write down the excitation table of *JK* and *D* flip-flop and derive the excitation equation for these two flip-flop.

   b) Draw logic diargam of the Master/Slave JK flip-flop. Why is it called so ?

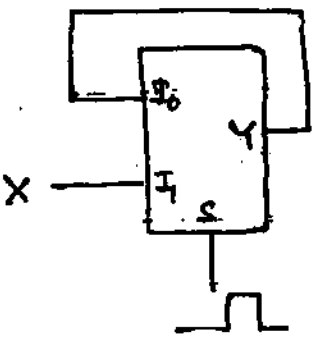
   c) Design a combinational circuit using an 8 × 4 ROM that accepts a 3-bit number and generates an output binary number equal to square of the input numbers.

(3 + 3) + 3 + 6

9. a) Prove that a Multiplexer is a universally complete logic module.

   b) Design a Full-subtractor using two 4-to-1 MUXs and other suitable gates.

   c) What will happen to the following circuit if the select(s) of the 2-to-1 MUX is driven by a clock, the output Y of the MUX is connected to the I_0 data input line and I_1 data input line is connected to X where X may be 0 or 1.



3 + 8 + 4

10. Write short notes on any *three* of the following : 3 × 5 = 15

   a) PLD

   b) Even parity generator and checker

   c) EPROM

   d) CMOS Logic

   e) Johnson counter.

END