Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (CSE)/SEM-8/CS-801D/2010

2010
VLSI DESIGN

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) Latches are generally

a) Level triggered b) Edge triggered

c) Both of these d) None of these.

ii) Which design rule is scalable in the context of VLSI design ?

a) λ rule b) χ rule

c) σ rule d) None of these.

iii) For pseudo-N MOS logic ratio of *Z* (pull-up) and *Z* (pull-down) is

a) 4 : 1 b) 3 : 1

c) 2 : 1 d) 1 : 1.

iv) In VHDL, default assignment value for a stable logic variable is

a) 0 b) 1

c) unsigned d) undefined.

v) One property of fuse-based FPGA is

a) one-time programmable

b) two-time programmable

c) three-time programmable

d) none of these.

vi) Approximate number of transistors in VLSI circuits is

a) < 20 b) < 200

c) ≤ 20,000 d) < 2,00,000.

vii) The basic length unit λ is about a few

a) μm b) *x*m

c) mm d) sq.m.

viii) The full form of ASIC is

a) Application Specific Integrated Circuit

b) Application Special Integrated Circuit

c) Application Special Integrated Chip

d) none of these.

ix) Which of the following devices is expected to have highest input impedance ?

a) BJT b) JFET

c) MOSFET d) Pn Jn.

x) A depletion MOSFET differs from a JFET because it has no

a) gate b) channel

c) Pn Jn d) Source.

xi) The source self-bias technique cannot be used for

a) JFETs

b) Enhancement MOSFETs

c) Depletion MOSFETs

d) MODFETs.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Compare between CMOS technology and BiCMOS technology.

3. Give CMOS implementation of an XOR gate.

4. Draw stick diagram of an XNOR gate and of a function A(B+C).

5. Explain how an MOS transistor works as a switch.

6. What is latch-up ? How is it prevented ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain the operation of a basic NMOS inverter.

b) Why is a depletion mode MOSFET used in place of a resistor as a pull-up in inverter circuit ?

c) What is a CMOS inverter ?

d) How does it differ from an NMOS inverter ?

6 + 6 + 1 + 2

8. a) What do you mean by pass transistors ?

   b) What are their advantages ?

   c) Show how the AND gate logic is achieved with N MOS pass transistor trap.

   d) What is super buffer ? Give the circuit diagrams of inverting and non-inverting N-MOS super buffer.

   2 + 2 + 5 + 2 + 4

9. a) Briefly describe three different techniques of FPGA.

   b) Briefly describe array based programmable logic design and implementation. 7 + 8

10. a) What are meant by Z (pull-up) and Z(pull-down) ?

    b) Derive the required ratio between Z (pull-up) and Z (pull-down) if an N MOS inverter is to be driven from another N MOS inverter. 3 + 12

11. Write short notes on any *three* of the following : 3 × 5

    a) Programmable logic array

    b) Inverter transfer characteristics

    c) FPGA

    d) Scaling in VLSI

    e) Ion-implantation process.