Name : ....

Roll No. : ....

Invigilator's Signature : ....

CS/B. TECH (CSE/IT)/SEM-3/EC-312/2010-11

2010-11
DIGITAL ELECTRONICS AND LOGIC DESIGN

Time Allotted : 3 Hours   *Full Marks* : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any ten of the following :

    $10 \times 1 = 10$

    i)   The race-around condition does not occur in Flip-Flop

         a)   J-K   b)   Master slave

         c)   T   d)   None of these.

    ii) A message bit is 010101. We are using even parity
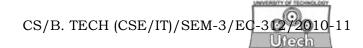   generator, so that the parity bit added to the message
         bit is

         a)   0   b)   1

         c)   0 & 1   d)   None of these.

iii) If, $(128)_{10} = (1003)_b$, the possible base b is

    a)   3   b)   4

    c)   5   d)   6.

iv) Which of the following codes is not a BCD code ?

    a)   Gray   b)   Xs-3

    c)   8421   d)   All of these.

v) $(11011)_2$ in BCD 8421 code is

    a)   00011011   b)   00100111

    c)   11011001   d)   01101100.

vi) In which code do the successive code characters differ in only one position ?

    a)   Gray   b)   Xs-3

    c)   8421   d)   Hamming code.

vii) The output of a gate is low if and only if all its inputs are high. It is true for

    a)   AND   b)   X-NOR

    c)   NOR   d)   NAND.

viii) The no. of rows in the truth table in the 4 input gate is

    a)   4   b)   8

    c)   12   d)   16.

ix) A bubbled AND gate is equivalent to a

a) OR gate   b) NAND gate

c) NOR gate   d) X-OR gate.

x) What is the minimum no. of NAND gates required to realize an X-OR gate ?

a) 3   b) 4

c) 5   d) 6.

xi) $A + A'B + A'B'C + A'B'C'D + \ldots \ldots =$

a) $A + B + C + \ldots$ b) $A' + B' + C' + D' + \ldots$

c) 1   d) 0.

xii) A code used for labelling the cells of a K-map is

a) 8-4-2-1 binary   b) Hexadecimal

c) Gray   d) Octal.

xiii) How many full adders are required to construct m bit parallel adder ?

a) $m/2$ b) $m-1$

c) m d) $m+1$.

xiv) A PLA is

a)   Mask programmable

b)   Field programmable

c)   Can be programmed by a user

d)   Can be erased and programmed.

xv) A carry look ahead adder is frequently used for addition because, it

a)   is faster   b)   is more accurate

c)   uses fewer gates   d)   costs less.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following.

$3 \times 5 = 15$

2. Convert J-K to S-R and J-K to T.

3. Explain Master Slave Flip-Flop.

4. Design MOD-10 synchronous counter and draw the timing diagram.

5. With the help of a block diagram, explain the working principle of a serial adder.

6. Define the following parameters of DACs :

   a) Resolution

   b) Offset error

   c) Monotonicity

   d) Settling error

   e) Percentage resolution.
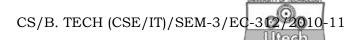
GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Simplify the following function by means of tabulation methods.

   $F (A, B, C, D) = \Sigma\, m\, (0, 1, 4, 7, 9, 11, 13, 15) + \Sigma\, d\, (3, 5)$

   b) Minimize the following expression using Karnaugh-map :

   i) $F(A, B, C, D) = \Pi M(0, 1, 3, 8, 10, 15) + \Pi d(11, 13, 14)$

   ii) $F(A, B, C, D) = \Sigma m(0, 4, 7, 9, 13, 15) + \Sigma d(10, 14)$

8. a) Implement the following function using 4:1 MUX only :

   $F (A, B, C, D) = \Sigma\, m\, (0, 2, 3, 6, 8, 9, 12, 14)$

b) Write down the excitation table of JK and D flip-flop and derive the excitation equation for these two flip-flops.

c) Design a 4-bit up / down asynchronous counter using all JK flip-flops and other necessary logic gates. Use one direction control input. If M = 0, the counter will count up and for M = 1, the counter will count down. 3 + 6 + 6

9. a) With the help of a necessary circuit diagram, explain the operation of dual slope ADC.

b) Distinguish between ROM, PLA and PLDs as elements realising Boolean function.

c) Find the conversation time of a successive approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference. What is the conversion rate ? 6 + 5 + 4

10. a) Design an n-bit full subtracter using full subtracter only and explain its operation.

b) Implement the BCD to Excess-3 code conversion using ROM.

c) Design a bi-directional shift registers and explain its operation. 4 + 5 + 6

11. Write short notes on any three of the following :   3 × 5

    a)   Even Parity Generator and Checker

    b)   SOP and POS canonical forms of binary subtraction

    c)   Johnson Counter

    d)   Priority Encoder

    e)   BCD adder

    f)   Flash memory

    g)   BCD to 7-segment decoder.

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