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Paper Code : CS-301

ANALOG AND DIGITAL ELECTRONICS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Parity generator is used for
   a) error detection b) amplitude detection
   c) noise detection d) none of these.

ii) Synchronous circuits change their state with
   a) input b) clock pulse
   c) output d) none of these.

iii) The efficiency of class *A* amplifier is
   a) 0.5 b) 1
   c) 0.25 d) 0.1.

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iv) Exclusive-OR (XOR) logic gates can be constructed from what other logic gates ?
   a) OR gates only
   b) AND gates, OR gates and NOT gates
   c) OR gates and NOT gates
   d) none of these.

v) If $(54)_{10} = (X)_4$, then the value of X is
   a) 123 b) 312
   c) 213 d) 132.

vi) $A + A'B + A'B'C + A'B'C'D +$ ..... equals.
   a) $A + B + C + D$ b) $A' + B' + C' + D'$
   c) 1 d) 0.

vii) The minimum number of NAND gates required to implement an EX-OR gate is
   a) 2 b) 3
   c) 4 d) 5.

viii) The net phase shift of Wien-bridge oscillator around the loop is
   a) 90° b) 180°
   c) zero d) 360°.

ix) $[AB'(C + BD) + A'B']C$ is
   a) AB' b) BC
   c) $B'C$ d) AB.

x) If the Q of a single stage single tuned amplifier is doubled, then bandwidth will
   a) remain the same b) become half
   c) become double d) become four times.

xi) Fastest logic gate family is

a) CMOS b) ECL

c) TTL d) RTL.

xii) The number of flip-flops required to design a Mod 10 counter is

a) 3 b) 4

c) 5 d) 6.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Implement the function of D flip-flop using J-K flip-flop.

3. Simplify the following functions using K-map :

a) $F(A, B, C, D) = \Sigma_m (7, 9, 10, 11, 12, 13, 14, 15)$

b) $F(A, B, C, D) = \pi_M (0, 2, 3, 6, 7) + \pi_d (8, 10, 11, 15)$.

4. Design a 5 : 32 decoder using 2 : 4 and 3 : 8 decoders.

5. Draw and explain the operation of monostable multivibrator using 555 timer.

6. Describe the working of S-R flipflop using truth table, logic diagram and excitation table.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Design a MOD 4 synchronous counter using J-K flip-flops and implement it.

b) Implement a full subtractor using demultiplexer.

c) Design a full adder using two half adders.

8. a) Design an asynchronous 3-bit up-down counter using J-K flip-flop which counts up when external signal $M = 1$ and counts down when $M = 0$.

b) With a neat circuit diagram, explain the operation of a 4-bit Johnson counter implemented using *D* flip-flop. 7 + 8

9. a) Draw and explain the master-slave J-K flip-flop using NAND gate.

b) Write down the excitation table and covert SR to JK flip-flop.

c) Describe the operation of a bi-directional universal shift register (with parallel load) with a neat diagram. 5 + 5 + 5

10. a) What are the conditions necessary for the generation of oscillation ?

b) Explain the operation of a Wien-bridge oscillator using Op-Amp with a circuit diagram.

c) Derive an equation for its frequency of oscillation.

d) What is Barkhausen criterion ? 2 + 5 + 5 + 3

11. Write short notes on any *three* of the following : 3×5

a) Parallel input serial output shift register

b) Decimal to BCD encoder

c) A/D converter using successive approximation

d) Asynchronous ripple counter

e) TTL family.