	Utech
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Invigilator's Signature :	

# CS/B.TECH (BME-OLD)/SEM-4/EC-405/2012 2012

#### **DIGITAL ELECTRONICS CIRCUIT**

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

#### **GROUP - A**

#### (Multiple Choice Type Questions)

1. Choose the correct alternatives for the following:

 $10 \times 1 = 10$ 

- The minimum no of NAND gates required to design one X-OR gate is
  - a) 4

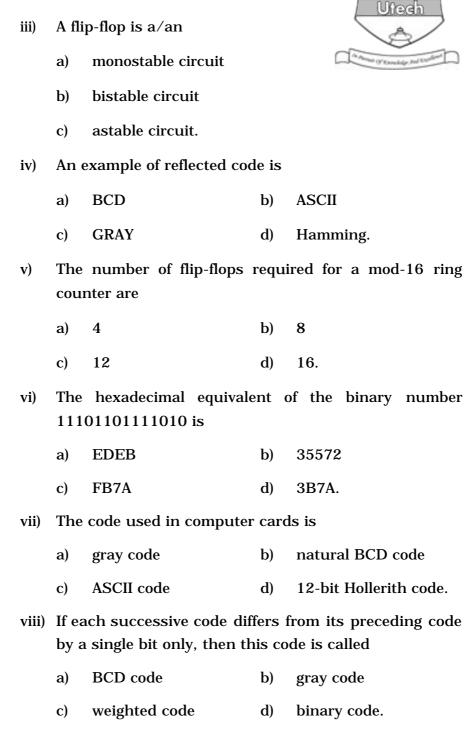
b) 5

c) 7

- d) 6.
- ii) The logic expression  $A\bar{B} + \bar{A}B$  can be implemented by giving inputs A & B to a two input
  - a) NAND gate
- b) X-OR gate
- c) NOR gate
- d) X-NOR gate.

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- ix) For a binary half substractor with inputs A & B, the correct logic expression for the output difference (D) and the borrow (X) are
  - a)  $D = AB + \overline{A}B$ ;  $X = \overline{A}B$
  - b)  $D = \bar{A}B + A\bar{B}$ ;  $X = A\bar{B}$
  - c)  $D = \bar{A}B + A\bar{B}$ ;  $X = \bar{A}B$
  - d)  $D = AB + \bar{A}B$ ;  $X = A\bar{B}$ .
- x) The characteristic equation of T flip-flop is given by
  - a)  $Q^+ = \overline{T}Q + T\overline{Q}$
- b)  $Q^+ = T\overline{Q} + \overline{T}Q$
- c)  $Q^+ = T\overline{Q}$
- d)  $Q^+ = TQ$ .

#### **GROUP - B**

## ( Short Answer Type Questions )

Answer any three of the following.

- $3 \times 5 = 15$
- 2. Draw and explain the construction of 2 input NAND gate with tristate logic of TTL logic family.
- 3. Simplify the following expression using the Karnaugh map.

$$X = B\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}D + \bar{A}BCD + ABCD.$$

- 4. What is Race around problem in flip-flops? How can it be avoided?
- 5. What are minterms? Simplify the expression by Boolean algebra

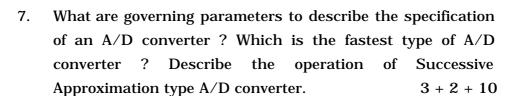
$$F = AB + \bar{A}C + A\bar{B}C (AB + C). \qquad 2 + 3$$

6. Construct a full subtractor with the use of multiplexer.



### ( Long Answer Type Questions)

Answer any *three* of the following.  $3 \times 15 = 45$ 



- 8. a) Realise a JK flip-flop ( clocked type ) with NAND gates.
  - b) Realise the following counter by D Flip-flop.

$$\rightarrow 0 \rightarrow 3 \rightarrow 2 \rightarrow 5 \rightarrow 7$$

- 9. Write short notes on any three of the following:  $3 \times 5$ 
  - a) Sequential circuit
  - b) CMOS TTL interfacing
  - c) Demultiplexer
  - d) Asynchronous state machine.
- 10. a) Explain the principle of operation of a parallel in serial out shift register with block diagram.
  - b) Design a 4-bit Bidirectional shift register.
  - c) Write down the application of shift register. 6 + 6 + 3
- 11. Explain the operation of a 4-bit Up-Down counter with its timing digram.