# Name : <br> Roll No. <br> $\qquad$ <br> $\qquad$ <br> CS/B.Tech (BME)/SEM-4/EC-405/2011 2011 <br> DIGITAL ELECTRONIC CIRCUITS 

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

## GROUP - A

( Multiple Choice Type Guestions )

1. Choose the correct alternatives for any ten of the following :
i) The hexadecimal equivalent of the binary number 11101101111010 is
a) EDEB
b) 35572
c) FB 7 A
d) 3 B 7 A .
ii) If $(212)_{x}=(23)_{10}$ where $x$ is base ( +ve integer ) then the value of $x$ is
a) 2
b) 3
c) 4
d) 5 .

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iii) The decimal equivalent of the binary ( $1110101 \cdot d 1$ ) is
a) $(17 \cdot 75)_{10}$
b) $(117 \cdot 75)_{10}$
c) $(217 \cdot 25)_{10}$
d) $(47 \cdot 81)_{10}$.
iv) The minimum number of NAND gates required to implement the Boolean function $A+A B^{\prime}+A B^{\prime} C$ is
a) zero
b) 1
c) 4
d) 7 .
v) The flip-flop, which is free from race around problem is
a) R-S flip-flop
b) Master-Slave flip-flop
c) J-K flip-flop
d) none of these.
vi) Which family has the better noise margin?
a) ECL
b) MOS
c) DTL
d) TTL.
vii) $D$ flip flop can be used as a
a) Divider circuit
b) Delay circuit
c) Differentiator
d) None of these.
viii) The memory which is UV erasable and electrically programmable is
a) EEROM
b) EPROM
c) PROM
d) RAM.
ix) The operation of the following circuit in the negative level logic system is

a) AND
b) OR
c) NAND
d) NOR.
x) In standard TTL, the "totem pole" stage refers to the
a) multi-emitter i/p stage
b) phase splitter
c) $\mathrm{o} / \mathrm{p}$ buffer
d) open collector o/p stage.
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a) XOR gates
b) NOR gates
c) NAND gates
d) OR gates.
xii) A flip-flop is a/an
a) monostable circuit
b) bistable circuit
c) astable circuit.
xiii) An example of reflected code is
a) BCD
b) ASCII
c) GRAY
d) Hamming.
xiv) The number of flip-flops required for a mod-16 ring counter are
a) 4
b) 8
c) 12
d) 16 .

2. What is fan out? what is the basic difference of a latch and edge triggered flip-flop ? Design a 9-bit even parity generator circuit.

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1+1+3
$$

3. Design BCD-Excess 3 code converter using basic logic gates with proper truth table.
4. What is Race Around condition ? Explain the working of Master-Slave Flip-Flop. $1+4$
5. Draw the neat diagram of a 4 bit Bi-directional Shift register using mode control ( $M$ ). When $M$ is logic zero then left shift and right shift for $M$ is logic one.
6. Using Quine-McCluskey method, minimise the following Boolean function $F=\sum m(0,1,5,7,8,11,13)$.

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7. a) Draw the timing diagram of MOD-10 counter where the MOD-10 counter is designed by cascading MOD-2 followed by MOD-5 counter units.
b) Design a sequential circuit that implements the following state diagram. Use all D-flip-flops.

8. a) What are the basic differences between SARM and DRAM ?
b) What is PLD ? Name different types of PLDs.
c) Realise the following three functions using a PAL :

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\begin{aligned}
& F_{1}(A, B, C, D)=\sum(1,3,8,5)+d(4,9) \\
& F_{2}(A, B, C, D)=\sum(1,3,9)+d(5,7,13) \\
& F_{3}(A, B, C, D)=\sum(2,7,8)+d(0,5,13)
\end{aligned}
$$

9. a) Define combinational logic circuit with example. How does it differ from a sequential logic circuit?
b) What is a full adder ? Design a full adder logic using two half adders and find the expressions for the sum and carry out. Also draw the logic circuit for a half subtractor. $\quad(2+2)+(2+7+2)$
10. a) Design a comparator using decoder with an active low outputs to compare two 2 -bit binary numbers. Other logic gates can be used in addition to the decoder. The outputs should show the greater than, less than and equal to output.
b) Gray code is a "Reflected Code". Explain. Draw the circuit to convert a 4-Bit Gray code to its binary. $\quad 10+3+2$
11. Write short notes on any three of the following :
a) Sequential circuit
b) CMOS TTL interfacing
c) Demultiplexer
d) Asynchronous state machine.
