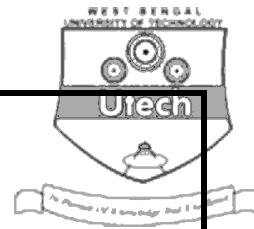
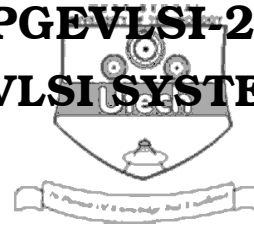
[illegible]

[ Full Marks : 30

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**CS/M.TECH (ME/VLSI )/SEM-2/PGEVLSI-204/09****TESTING & VERIFICATION OF VLSI SYSTEMS****SEMESTER - 2**Time : 1  $\frac{1}{2}$  Hours ]

[ Full Marks : 30

**GROUP – A**( Answer any *one* question )

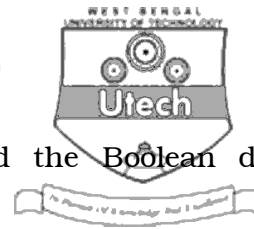
1 × 10 = 10

1. a) Explain the concept of state machine representation using Binary decision diagrams. Show the steps of converting the state machine description to an equivalent ROBDD representation. 8
- b) State the application of BDDs in verification. 2
2. Which of the following are *true* / *false* ? Give short reasons : 5 × 2 = 10
  - a)  $G(p)$  is equivalent to  $F(\neg p)$ .
  - b) The size of ROBDD of  $(a1 \wedge b1) \vee (a2 \wedge b2)$  for the variable ordering  $(a1 < a2 < b1 < b2)$  is lesser than one generated for the same function ordering  $(a1 < b1 < a2 < b2)$ .
  - c) A Boolean formula is satisfiable implies that the formula is always true.
  - d) Two Boolean functions are equivalent if they have the same ROBDD representation for the same variable ordering.
  - e) Circuits with combinational loops cannot be simulated with cycle based simulation.



**GROUP – B**

( Answer any *two* questions )



2 × 10 = 20

3. a) Consider the logic circuit shown below. Find the Boolean difference with respect  $x_2$  . 4

dia

- b) Explain with flowchart, the PODEM algorithm for test generation for combinational logic circuits. 6
4. a) What are the properties of a testable circuit ? How is testability achieved ? 2
- b) What is controllability and observability ? 1
- c) What is scan design ? Explain in brief the rules of scan design. 3
- d) Describe a BIST implementation method. 4
5. a) Draw the schematic of an integrated circuit with 1149.1 boundary scan standard. What is a boundary register ? What is a boundary register cell ? 6
- b) Draw the tap controller timing diagram and explain the function of IDCODE and USER CODE instructions. 4

END