CS/M.TECH (ME/VLSI)/SEM-2/PGEVLSI-204/09
TESTING & VERIFICATION OF VLSI SYSTEMS (SEMESTER - 2)

1. ..... *Signature of Invigilator*

2. ..... *Signature of the Officer-in-Charge*

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

CS/M.TECH (ME/VLSI)/SEM-2/PGEVLSI-204/09
ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009
TESTING & VERIFICATION OF VLSI SYSTEMS (SEMESTER - 2)

Time : $1\frac{1}{2}$ Hours] [Full Marks : 30

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. You have to answer the questions in the space provided marked 'Answer Sheet'. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

---

FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

Question Number											***Total Marks***	***Examiner's Signature***
Marks Obtained												

.....
Head-Examiner/Co-Ordinator/Scrutineer

48015 (08/07)

DO NOT WRITE ON THIS PAGE

CS/M.TECH (ME/VLSI)/SEM-2/PGEVLSI-204/09

TESTING & VERIFICATION OF VLSI SYSTEMS

SEMESTER - 2

Time : $1\frac{1}{2}$ Hours] [Full Marks : 30

GROUP – A

(Answer any *one* question) 1 × 10 = 10

1. a) Explain the concept of state machine representation using Binary decision diagrams. Show the steps of converting the state machine description to an equivalent ROBDD representation. 8

   b) State the application of BDDs in verification. 2

2. Which of the following are *true* / *false* ? Give short reasons : 5 × 2 = 10

   a) $G\ (\ p\ )$ is equivalent to $F\ (\ \neg\ p\ )$.

   b) The size of ROBDD of $(\ a1 \barwedge b1\ ) \vee (\ a2 \barwedge b2\ )$ for the variable ordering

   $(\ a1 < a2 < b1 < b2\ )$ is lesser than one generated for the same function ordering $(\ a1 < b1 < a2 < b2\ )$.

   c) A Boolean formula is satisfiable implies that the formula is always true.

   d) Two Boolean functions are equivalent if they have the same ROBDD representation for the same variable ordering.

   e) Circuits with combinational loops cannot be simulated with cycle based simulation.

GROUP – B

(Answer any *two* questions) 2 × 10 = 20

3. a) Consider the logic circuit shown below. Find the Boolean difference with respect x_2 . 4

dia

b) Explain with flowchart, the PODEM algorithm for test generation for combinational logic circuits. 6

4. a) What are the properties of a testable circuit ? How is testability achieved ? 2

b) What is controllability and observability ? 1

c) What is scan design ? Explain in brief the rules of scan design. 3

d) Describe a BIST implementation method. 4

5. a) Draw the schematic of an integrated circuit with 1149·1 boundary scan standard. What is a boundary register ? What is a boundary register cell ? 6

b) Draw the tap controller timing diagram and explain the function of IDCODE and USER CODE instructions. 4

END