Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (ECE-VLSI)/SEM-2/MVLSI-201/2013

2013

PROCESSOR ARCHITECTURE FOR VLSI

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Objective Type Questions)

1. Answer the following questions briefly : 10 × 1 = 10

   i) What do you mean by precision and range of floating point numbers ?

   ii) Describe Intel Hex File Format (.HEX) for translating Object File (.OBJ) created by an assembler into.

   iii) What is the difference between fixed point and floating point DSPs ?

   iv) What is multichannel buffered serial port (McBSP) in connection with TMS320C50 processor ?

   v) IBM PowerPC is a power optimized enhanced RISC processor. Explain this statement.

vi) Why is backward compatibility less important in an embedded device than in a general purpose device ?

vii) What do you mean by VLIW architecture ?

viii) Discuss features of pipelining in embedded processor in contrast to traditional processor.

ix) Highlight IEEE standard double precision floating point format for embedded computation.

x) Compare von Neumann and Harvard architecture of a processor based system.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What are the functions of Barrel Shifter and MAC Unit of TMS320C6X family of DSPs ?

3. Explain the architecture of Configurable Logic Block (CLB) widely used in programmable logic devices.

4. CISC processors generally have better code density than the RISC processors, but thumb instructions of ARM processor offer better code density than many CISC processors. Explain with reasons.

5. Why are phase locked loop (PLL) resources integrated with DSP processors ? Explain clearly with example, if any.

6. Illustrate the basic computations involved in an FIR Filter and suggest an optimized Digital Hardware for the same. Do you think that this Hardware is readily available in a Digital Signal Processor (DSP) ? Explain.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. Explain briefly the architecture of ARM processor with a block schematic representation. Also briefly highlight the features of ARM programming model.

8. Explain the advanced multi-bus architecture of TMS320C50 Digital Signal Processor (DSP) and highlight the salient features of the Computational Block of the processor. Explain the essential features of VLIW architecture.

9. Explain briefly the architecture of IBM PowerPC processor with a block schematic representation.

10. Explain the architectural features adopted in Microchip PIC18f452 family of processors. Also highlight the essential on-chip resources for embedded computation.

11. a) Highlight the major issues of pipelining related to processor design trade-offs between CISC and RISC based on the dynamic usage statistics of instructions on a functional classification in a typical application program. 10

    b) All instructions in ARM processor are conditional. Explain the advantages of such features of ARM processor in contrast to generic processor. 5

12. Write short notes on any *three* of the following : 3 × 5

    a) Pipeline hazards in RISC processors

    b) Dual Access Ram (DARAM)

    c) Soft Core Processor

    d) IEEE floating point format for embedded computation

    e) Memory organisation in ARM processor

    f) Architectural features to support RTOS implementation.