Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH (ECE-VLSI)/SEM-2/MVLSI-205B/2013

2013

LOW POWER VLSI DESIGN

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* of the following : 5 × 14 = 70

1. a) Write the expression for different components of power dissipation in CMOS integrated circuit.

   b) Why low power VLSI design is important ?

   c) Derive a mathematical expression and explain with a block diagram how parallel architecture with voltage scaling helps to reduce power dissipation in low power VLSI design. 4 + 2 + 8

2. a) What do you mean by signal probability ? Given $y = x_1 x_2 + x_1 x_3$, where x_1, x_2 and x_3 are mutually independent. Compute the signal probability $P(y)$.

   b) What do you mean by switching activity ? Write the different techniques to reduce the switching activity of a CMOS circuit. 1 + 4 + 2 + 7

3. a) Using schematic cross-section, explain the leakage power dissipation of a static CMOS inverter. How variable threshold helps to reduce sub-threshold leakage current ?

   b) Draw the block diagram of a typical low power chip based on variable-threshold CMOS circuits and explain its operation. 6 + 3 + 5

4. a) Explain the principle of adiabatic logic circuit for low power design.

   b) How logic encoding helps to reduce power consumption ?

   c) Describe the principle of signal gating for low power design. 5 + 5 + 4

5. a) Explain three major sources of power consumption in a memory chip.

   b) Explain the principle of a six-transistor SRAM cell.

   c) Write the different techniques to reduce power dissipation in clock networks. 4 + 5 + 5

6. a) What is signal entropy ? Explain the method of power estimation using entropy.

   b) Explain different techniques of software power estimation. 2 + 5 + 7

7. a) How the size of transistor and gate affect the amount of power dissipation in CMOS circuit ?

   b) Explain how voltage scaling helps to reduce power dissipation in a CMOS integrated circuit.

   c) What do you mean by glitch ? How power dissipation due to glitch can be reduced ? 5 + 4 + 5

8. Write short notes on any *two* of the folloiwng : 2 × 7

   a) Power reduction employing operator reduction

   b) Pass Transistor Logic circuits for low power design

   c) Multi-threshold CMOS circuits

   d) Pre-computation logic.