Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(ECE-VLSI)/SEM-2/MVLSI-203/2012

2012
ANALOG IC DESIGN

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *four* from the rest.

1. a) In Fig. 1, calculate the minimum output voltage required to keep the device in saturation. 2

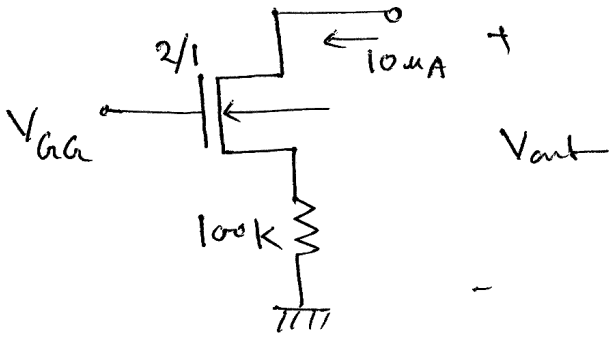

Fig. 1

b) How threshold voltage of MOSFET shifts due to body bias effect ? 2

c) How NMOS transistor can be used as linear resistor ? 2

d) For CMOS push-pull inverter shown in Fig.2, find the small signal voltage gain A_v if $I_D = 200\mu A$, $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{5\ \mu m}{1\ \mu m}$, $C_{gd_1} = C_{gd_2} = 5fF$, $C_{bd_1} = C_{bd_2} = 30fF$ and $C_L = 10PF$. 2

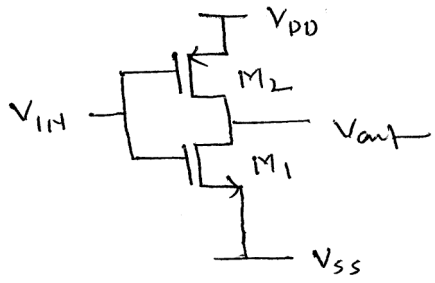

Fig.2

e) What is clock feed-through ? 2

f) Explain one advantage and one disadvantage of depletion type NMOS over enhancement type NMOS device. 2

g) Calculate the intrinsic gain of an NMOS device operating in saturation with $\frac{W}{L} = \frac{50}{0 \cdot 5}$ and $|I_D| = 0 \cdot 5$ mA. 2

2. Explain common source single stage amplifier with source degeneration. How does common gate stage differ from common source stage ? Derive and calculate the voltage gain of a common gate stage with a current source load as shown in Fig. 3. Explain the circuit operation of folded cascade stage.

4 + 2 + 4 + 4

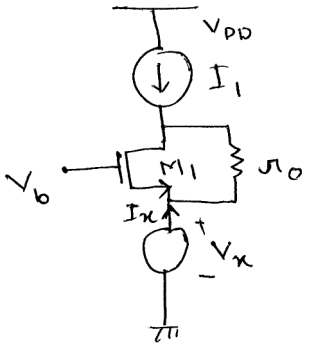

Fig . 3

3. a) What is differential pair ? Derive and explain quantitative analysis of basic differential pair circuit.

2 + 6

b) A differential pair uses input NMOS devices with $\frac{W}{L} = \frac{50}{0 \cdot 5}$ and tail current of 1mA.

(i) What is the equilibrium overdrive voltage of each transistor ?

(ii) How is the tail current shared between the two sides if $V_{in_1} = V_{in_2} = 50\text{mA}$? 3 + 3

4. Explain basic concepts and performance parameters of CMOS operational amplifier. Explain the MOS two-stage operational amplifier in detail. What are the various referenced biasing techniques used in the MOSFET ?

4 + 6 + 4

5. What is DAC ? Explain $\frac{D}{A}$ conversion principle in detail. What are the basic parameters and terminologies associated with the performance of practical $\frac{D}{A}$ converter circuits ? Explain flash type ADC. 1 + 6 + 4 + 3

6. What do you understand by "switched capacitor" ? Explain basic switched capacitor operation in detail. Give detail explanation about switched capacitor integrator. 2 + 6 + 6

7. Derive and explain fundamental concept of N-channel current mirror. What are the applications of ideal current and voltage references in analog circuit design ? Fig. 4 illustrates a reference circuit that provides a reference voltage output. Derive a symbolic expression of V_{ref}. Draw and explain Wilson-current mirror. What are the basic differences between Wilson-current mirror and cascade current mirror ?

3 + 2 + 3 + 4 + 2

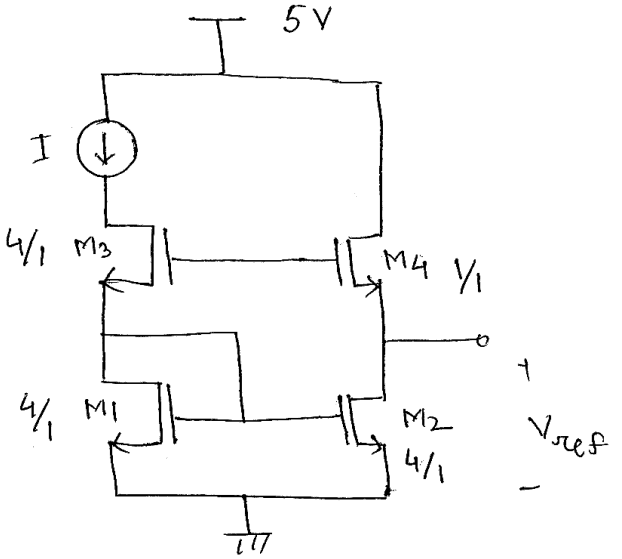

Fig. 4

8. What do you understand by PLL ? Explain the principle of operation of PLL system. Explain capture phenomenon and tracking characteristics of PLL in detail. Explain the operation of VCO with neat diagram. 2 + 4 + 5 + 3