Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (VLSI)/SEM-2/PGMVD-204A/2010

2010

ADVANCED MICRO AND NANO DEVICES

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

1. Answer briefly any *five* of the following question : 5 × 2 = 10

   i) Why is CMOS particularly suitable to meet the stringent requirements of the performance of a VLSI chip ?

   ii) What are the parasitic resistances present in a MOSFET ? Show with a diagram.

   iii) What are the different components of the parasitic overlap capacitance in a MOSFET ?

   iv) What is the advantage of multiple fringe GATE MOS ?

   v) Which properties of the Quantum Well Laser make it superior in performance compared to the bulk Laser ?

vi) $Al_xGa_{(1-x)}As/GaAs$ heterostructure devices are the most studied heterostructure. Justify.

vii) Nano Porous Silicon gives photoluminescence whereas Semiconducting Si cannot. Explain.

viii) What is RHEED system ? What is its use in Molecular Beam Epitaxy ?

ix) Comment on the Density of State function (DOS) in bulk material and in quantum well heterostructures.

x) What is lattice misfit factor of an epitaxial film ? How does the critical layer thickness of an epitaxial film control the device properties ?

GROUP – B

Answer any *two* of the following. 2 × 5 = 10

2. Why does *p*-MOS of the CMOS circuit have wider channel than the *n*-MOS ? What is the choice ratio of *p*-MOS channel width to *n*-MOS channel width in sub-micron CMOS technology ? 3 + 2

3. Define the different channel lengths which are the key parameters of CMOS technology. Explain their significance. 5

4. What is the goal of the Silicide technology and how does it achieve it ? 2 + 3

Answer any *two* of the following : 2 × 15 = 30

5. An input step-function is applied to a CMOS inverter. Set up the equation for the pull-down and pull-up switching characteristics. Hence define the terms *n*-MOS pull-down delay and *p*-MOS pull-up delay. Under what condition will the two delays be the same ? Describe how the energy is dissipated during a switching cycle. What is the energy that irreversibly lost ? What is the peak power dissipated ? Why does the average power depend on switching rate ?

   4 + 1 + 1 + 1 + 4 + 2 + 1 + 1

6. How does the parasitic capacitance originate in the VLSI chip due to the interconnect ? Explain with diagram. How can the packing density of modern VLSI chips be improved ? What are the scaling rules for the 'interconnects' ? What is the overall effect of scaling on the RC delay of the 'interconnects' ? What happens to the current density ? Can global wires be scaled down like the local wires ? Justify your statement. How can this problem be overcome ? 3 + 1 + 3 + 3 + 1 + 2 + 2

7. What are the inherent advantages of the SOI device over the bulk device ? What are Partially Depleted (PD) and Fully Depleted (FD) SOI MOSFETs ? Explain with suitable diagram. Discuss the relative merits and demerits. How does the Heterojunction FET help in providing higher switching speed ? 3 + 4 + 4 + 4

GROUP – C

Answer any *one* of the following. 1 × 5 = 5

8. What is meant by "epitaxy" ? How heteroepitaxy is different from homoepitaxy ? What causes do strain in epitaxial layer ? 1 + 2 + 2

9. What are the advantages of using metal alkyls as precursor materials in MOCVD growth technique ? Write the overall surface reaction for the growth of GaAs layer in this technique. 3 + 2

Answer any *one* of the following. 1 × 15 = 15

10. How can you distinguish MOCVD from conventional CVD ? What materials are generally used as *n*-type and *p*-type dopants for the growth of III-V compounds in MOCVD process ? Why is rigorous safety precaution necessary in MOCVD process ?

    Draw the schematic diagram for a typical MBE reactor. The substrate in the reactor needs moderately high temp. for the growth process. Explain. Mention the advantages and disadvantages of the MBE technique.

    2 + 2 + 1 + 4 + 2 + 2 + 2

11. What is meant by "Capacitance-Voltage" measurement ? Draw the typical C-V characteristics of an ideal MOS capacitor. Mark the individual capacitance components on the characteristics and explain briefly the origin of the components. How the C-V characteristics can be a function of the frequency of the ac signal used to measure the capacitance ? The experimental C-V curve can be used as a diagnostic tool in MOS device process control. Justify. 2 + 2 + 6 + 2 + 3