



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS/M.TECH(VLSI)/SEM-1/PGMVD-102/2012-13**

**2012**

**PHYSICS OF VLSI DEVICES**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP – A**

**( Objective Type Questions )**

1. Answer any *ten* of the following : 10 × 1 = 10
- i) Why does a MOSFET have higher input impedance than a BJT ?
  - ii) How is the threshold voltage of an ideal MOSFET modified for a real MOSFET ?
  - iii) Write down the voltage balance equation for a MOS capacitor.
  - iv) Mention any two sources of parasitic charge present in the oxide layer of a MOSFET.
  - v) Write down the charge balance equation of a MOSFET.
  - vi) What is the surface voltage value at the point when the channel gets inverted ?



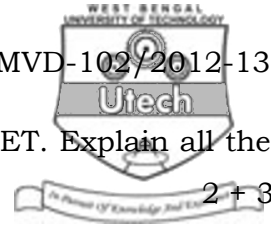
- vii) How can the Gate charge of a two-terminal MOS structure be balanced ?
- viii) What is body effect in a three-terminal MOSFET ?
- ix) Why does  $p$ -MOS of the CMOS circuit have wider channel than the  $n$ -MOS ?
- x) What does the Transconductance of a MOSFET signify ?
- xi) When will a MOSFET show Short Channel Effects ?
- xii) Why is BiCMOS preferred to CMOS ?
- xiii) What happens to the threshold voltage of an E-MOS when the source-body junction is reversed biased ?
- xiv) Mention one advantage of the BiCMOS over the CMOS.
- xv) How you can incorporate a resistor in a VLSI chip ?

**GROUP – B**

**( Short Answer Type Questions )**

Answer any *three* of the following  $3 \times 5 = 15$

- 2. A two-terminal MOSFET can be used as a capacitor. Why ? How does this capacitor vary with Gate-body voltage ? Explain with necessary diagram.  $1 + 2 + 2$
- 3. What do you mean by Noise margin of a CMOS inverter ? Which is the best choice for this Noise margin ? How can you improve the design of a CMOS chip to achieve this end ?  $1 + 2 + 2$
- 4. What are the different parasitic overlap capacitances in a MOSFET ? How are they formed ? Explain with a diagram.  $2 + 2 + 1$



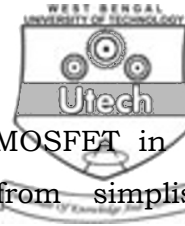
5. Draw the DC equivalent circuit of a MOSFET. Explain all the parameters. 2 + 3
6. What are the different models for the device design for VLSI chips ? Which one you would prefer for statistical modelling ? Why ? 3 + 1 + 1

**GROUP - C**

**( Long Answer Type Questions )**

Answer any *three* of the following. 3 × 15 = 45

7. What are different domains of VLSI design ? "Behavioural Domain design has only one solution while Structural Domain design has multiple options." Explain. What is the Y-chart for VLSI design ? Elucidate. Discuss the different steps of VLSI design with suitable flow-chart. 3 + 2 + 2 + 2 + 4 + 2
8. What are the assumptions of an ideal MOSFET ? Write down the IDEAL Poisson's equation for computation of the channel charge and depletion width. How will the assumptions get modified in order to realize the realistic situation that includes both depletion and inversion ? What is the modified Poisson's' equation ? What is the need for the Flat-band voltage ? What is the relation between the Gate voltage and the flat-band voltage in order to induce a channel ? Draw the energy band diagrams for a *n*-type E-MOSFET for gate voltage less than, equal to, and greater than the flat band voltage. 2 + 1 + 2 + 1 + 2 + 2 + 5



9. Derive the current-voltage relations for a MOSFET in the saturation and non-saturation regions from simplistic considerations. Write down the starting expressions for the drift and diffusion components of the Drain-source current. When will each of these components dominate and why ? How can you find the inversion charge ?

3 + 3 + 2 + 2 + 2 + 3

10. a) Draw the equivalent circuit for the *ac* response of an E-MOSFET. Arrive at the necessary functional relationships needed for the equivalent circuit. Explain each of the circuit components and their significance.
- b) What are the different Short Channel Effects ?

( 2 + 4 + 4 ) + 5

11. a) What is Stick diagram ? Draw the Stick diagram for a NAND circuit.
- b) What are the different scaling methods that you may adopt for scaling down the VLSI chip ? Which one would be most effective in countering the problems of Short Channel Effects ? Justify. How would the different parameters scale in this case ?

( 2 + 3 ) + ( 3 + 1 + 3 + 3 )

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