Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (MC-VLSI)/SEM-1/PGMVD-105/2011-12

2011

DIGITAL VLSI CIRCUITS AND SYSTEMS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *five* questions taking at least any *two* from each Group.

GROUP – A

1. a) What are the advantages of CMOS logic gates over the BJT based gates ? 2

   b) How a resistor can be made using a MOS transistor ? 1

   c) Give CMOS circuits for the following : 3 + 4

      i) $y = \left(AB^{l}C + A^{l}BC^{l}\right)$

      ii) Sum and carry for a full adder.

   d) Explain why CMOS logic circuits consume very little power. 2

   e) Show the circuit of a pseudo *n*MOS inverter. 2

2. a) Give the logic expression for an AOI gate. Draw its transistor level equivalent. Draw its stick diagram. 2 + 2

b) Give the expression for calculating delay in CMOS circuit. 2

c) What happens to delay if you increase load capacitance ? 2

d) What happens to delay if we include a resistance at the output of a CMOS circuit ? 2

e) What are the limitations in increasing the power supply to reduce delay ? 2

f) What are the basic differences in design between FPGA and ASIC ? 2

3. a) Show how a tri-state buffer can be implemented using "pass transistor" ? What is its drawback ? Giving a circuit diagram, show how this drawback can be eliminated. 2 + 1 + 2

b) Give the MOS circuit of a non-restoring tri-state buffer. What are its advantages ? 3 + 1

c) Show how a 4 : 1 multiplexer can be implemented using tri-state buffers. 3

d) Show how a flip-flop can be designed using two NOT gates and two pass transistors. 2

4. a) Give the architecture of a 4 × 2 bit static RAM. Show the C-MOS circuit of a single cell. What do you mean by memory access time ? 5 + 2 + 1

   b) What is two-dimensional memory design ? Discuss clearly and indicate its advantages. 4

   c) Show the CMOS circuit of a single cell of a dynamic memory. 2

GROUP – B

5. a) Write down the steps involved for VLSI design cycle and explain the purpose of each step. 8

   b) What are the needs of the CAD tools ? 2

   c) What do you mean by lay out synthesis ? 2

   d) Explain why FPGAs are normally used for proto-type development of any VLSI chip. 2

6. a) What are the advantages of dynamic logic over the static CMOS logic ? 3

   b) With a circuit diagram, clearly explain the operation of dynamic logic. 4

c) How the drawbacks of 'static CMOS' circuits can be overcome by dynamic logic circuits ? For implementing an N input NAND using 'dynamic logic' how many MOS transistors will be required ? 2 + 2

d) What is the major problem in dynamic logic circuit ? Explain clearly. 3

7. a) With a circuit diagram, explain how cascading can be made possible in 'domino logic'. 3

b) Using 'domino logic', give the logic circuit of $\left(A.B^{l} + A^{l}.B\right).(C.D)$ where A, B, C, D are logic variables. 3

c) What is layout diagram ? How does it differ from stick diagram ? Show the layout diagram of an inverter and indicate the spacing. $1\frac{1}{2} + 1\frac{1}{2} + 3$

d) What is 'standard cell' library ? 2

8. a) Show the architecture of a FPGA and indicate its basic blocks. Explain clearly the operation of FPGA and show how it offers flexibility. 5 + 5

b) Giving a circuit diagram, show how a FPGA can be configured from the bit-stream stored in Flash Memory. 4