Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (ECE-VLSI)/SEM-1/MVLSI-103/2012-13

2012
DIGITAL IC DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *four* from the rest.

1. Answer the following questions briefly : 7 × 2

   a) What do you understand by "Port Map" ?

   b) Make layout for the function F = A + BC using Gate Array design.

   c) What is test bench and why is it needed ?

   d) What is technology mapping ? Explain with suitable example.

   e) What is high level synthesis ?

   f) What are the main advantages of using an FPGA for semi-custom VLSI design ?

   g) Design a CMOS half-adder circuit.

2. Explain Hardware Description Language (HDL). What is entity and what are the primary constructs of entity ? Explain RTL. What are the four different modelling styles of VHDL architecture ? Write VHDL code for full-adder using dataflow modelling style. Write behavioural VHDL code for n-bit serial adder. 2 + 3 + 1 + 2 + 3 + 3

3. What is ASIC ? How is ASIC different from general purpose IC ? Differentiate full-custom ASIC with respect to semi-custom ASIC. Explain semi-custom ASIC design flow in detail. 1 + 2 + 3 + 8

4. a) Explain dynamic logic. What are the advantages and disadvantages of dynamic logic over static logic ? What is charge sharing ? What are the techniques employed to minimize charge sharing in dynamic logic ?

   1 + 2 + 1 + 2

   b) Explain DCVSL. Using minimum number of transistors implement f & $\overline{f}$ in DCVSL. Assume a, b, c, d and their complements are available as inputs –

   $f = abc + acd$ 2 + 6

5. What is logic synthesis ? What are the constraints applied during logic synthesis ? What is the difference between technology-independent logic synthesis and technology mapping ? Name the different popular commercial tools available for logic synthesis. How is logic synthesis different from high level synthesis ? 2 + 2 + 3 + 4 + 3

6. a) What is physical design ? Make physical design for CMOS full-adder. 1 + 4

   b) What is partitioning ? What are the different levels of partitioning ? 1 + 3

   c) What is floor planning ? What are the major tasks in floor planning ? 1 + 4

7. Write short notes on the following : $4 \times 3\frac{1}{2}$

   a) CPLD

   b) Sea-of-gate design

   c) NORA logic

   d) VLSI design metrics.