Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(ECE)VLSI/SEM-1/MVLSI-103/2012-13

2012

DIGITAL IC DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Objective Type Questions)

1. Answer the following questions :

   i) Find the dual and complement of $F = A\,(B + C)$. Mention an application of the dual of a function.

   ii) Distinguish between a ratioed and ratioless inverter.

   iii) Draw a pseudo-NMOS load NOR2 gate and briefly mention the advantages and disadvantages.

   iv) An N-MOS passes a strong '0' and P-MOS passes a strong '1'. Explain.

   v) Write a VHDL programme of 32 bit adder using structural modelling style. 3 + 2 + 2 + 3 + 4

GROUP – B

(Long Answer Type Questions)

Answer any *four* of the following. 4 × 14 = 56

2. What are RTL, Gate, Metal and FIB fixes ? What are DRC and LVS ? Explain briefly. What are the tools provided in a modern EDA software packages ? 4 + 5 + 5

3. What do you mean by HDL ? How many hardware models are present in VHDL ? Briefly discuss the proper example of various hardware modelling in VHDL. What do you mean by Top down design and Bottom up design styles ? 1 + 1 + 8 + 4

4. Design a pseudo-NMOS inverter to deliver, $V_{OH} = V_{DD} = 1 \cdot 8\,\text{V}$ and $V_{OL} = 0 \cdot 05\,\text{V}$. Use the following parameters,

   $\mu_n = 270$ cm^2/V-S, $\mu_p = 70$ cm^2/V-S, $C_{OX} = 1 \cdot 0$ μF/cm^2,

   $V_{sat} = 8 \times 10^6$ cm/s, $V_{TN} = 0 \cdot 5$ V, $V_{TP} = -0 \cdot 5$ V,

   $E_{CN} L = 1 \cdot 2$ V, $E_{CP} = 4 \cdot 8$ V, $L = 200$ nm.

5. How are precharge and evaluate signals used in dynamic logic working ? Explain clearly. What problem arises in cascading such stages and how is it removed ? 8 + 6

6. Explain how a Transmission Gate is realized using a pair of NMOS and PMOS devices. What is the approximate value of the ON- resistance of the combination and why ? 8 + 6

7. Why we need CAD tools ? Briefly discuss about Placement, Floor planning and Routing. Why are they needed ? Draw the figure of a PLA, where $F_1 = xy + x'z$; $F_2 = y' + x'z$ and $F_3 = xy + y'z$. 1 + 8 + 5

8. Explain the advantages of CPL over Transmission Gates. Draw a neat diagram of a CPL based XOR gate and explain its working with particular reference to the level restoring PMOS gates. 4 + 10

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