*Name* : .....

*Roll No.* : .....

*Invigilator's Signature :* .....

**CS / M.TECH (VLSI) / SEM-1 / MVLSI-103 / 2010-11**

**2010-11**

# ADVANCED DIGITAL INTEGRATED CIRCUIT DESIGN

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

*Answer Q.No.1 and any four from the rest.*

## GROUP – A

## ( Short Answer Type Questions )

1. Answer any *seven* questions : 7 × 2

   i) What is 'keeper ckt' ? Draw and explain.

   ii) Differentiate between software simulators and hardware emulators.

   iii) What is meant by the strength of a gate ? Give an example of a weak gate.

   iv) What is critical path ?

   v) State the steps in a synthesis procedure.

   vi) What is the function of an Arbiter ?

vii) State the differences between high-level synthesis, logic synthesis and physical synthesis.

viii) What was the motivation for using asynchronous circuits ?

ix) Define the term 'O($n^2$) time complexity'.

x) What are the inputs and outputs of the placement procedure ?

**GROUP – B**

**( Long Answer Type Questions )**

Answer any *four* of the following. $4 \times 14 = 56$

2. a) Explore the different factors limiting the size reduction of CMOS devices.

b) What is 'one-hot encoding' ? Clarify the advantages and disadvantages. 7 + 3 + 4

3. a) What is clock skew ? How is it controlled ?

b) Explain qualitatively the 'genetic algorithm' as applicable to placement.

c) What types of design information do the following formats carry? 5 + 6 + 3

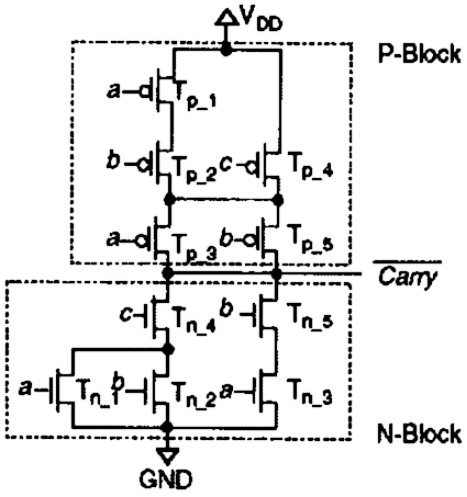
SDF, EDIF, GDSII

4. a) What is the problem with domino logic ?

b) Clarify with Generic structure of NORA logic circuit how the problem is overcome.

c) What is 'hardware accelerated simulation' ? 4 + 7 + 3

5. a) Optimize the circuit for equal rise and fall times :

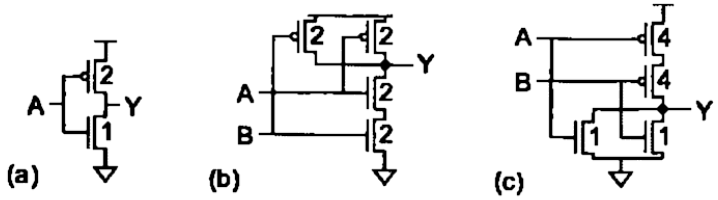



b) Draw and explain a CAM-structure with its operation and application. 5 + 9

6. a) What are the various sources of parasitic capacitances, inductances and resistances in a VLSI circuit ?

b) Draw and explain the two-phase routing flow.

c) Calculate the logical efforts of the gates shown :




5 + 5 + 4

7. a) What are the various timings associated with a circuit performance ? Explain.

b) Draw the binary tree of the following Boolean equation and reduce it to ROBDD.

$$f = \bar{x}_1 x_2 x_3 + x_1 \bar{x}_2 x_3 + x_1 x_2$$

c) What are the advantages and disadvantages of TG ? Design a mux using TG. 5 + 3 + 3 + 3

8. a) What are the different types of scaling ? Compare them.

b) Implement an order in a PGCA.

c) Construct a stick diagram of a single-bit full-adder by first drawing its transistor schematic. 6 + 3 + 5

==========