Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE)VLSI/SEM-1/MVM-103/2009-10

2009

ADVANCED DIGITAL INTEGRATED CIRCUIT DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *four* from the rest. 5 × 14 = 70

1. Justify the statements. Answer *all* questions : 7 × 2

   i) Positive surface potential applied to a *P* type MOS causes the energy band to bend near the surface.

   ii) An SRAM has maximum potential energy at its unstable point of its characteristic curve.

   iii) Constant voltage scaling is advantageous over constant field scaling.

   iv) Considering speed for memory buffer latch is faster than differential amplifier.

   v) To overcome charge sharing problem bootstrap capacitance is used.

   vi) Standard CMOS gates dissipate less power than its corresponding pseudo-NMOS counterparts.

vii) Justify the circuit as a Tristate Buffer.

2. a) What is narrow-channel effect ?

b) Consider a simple reverse biased abrupt *p-n* junction.

The doping density on *n*-type region is $N_D = 10^{19}$ cm^{-3} and doping density of the *p*-type region is $N_A = 2 * 10^{15}$ cm^{-3}. Sidewall (P^+) doping $N_A(\text{sw}) = 4 * 10^{16}$ cm^{-3}. Gate oxide thickness is 45 nm. Junction detpth is 1 μm. Calculate combined equivalent drain to substrate junction capacitance.

4 + 10

3. a) Describe the effect on the threshold voltage due to short channel effect.

   b) Consider a resistive load inverter with V_{DD} = 5V, kn = 20 μA/V^2 , V_{TO} = 0·8 V, R_L = 200 kΩ and W/L = 2. Calculate the critical voltage on the VTC and find the noise margins of the circuit.

   c) Describe the effect of supply voltage scaling in resistive load inverter. 5 + 7 + 2

4. a) Determine the low output voltage of a three input depletion load NOR gate.

   b) Discuss the transient analysis of a two input XOR gate. 8 + 6

5. a) Describe the operation of a clocked JK flipflop with proper timing diagram.

   b) Considering power, is CPL advantageous over CMOS logic ?

   c) Describe basic principle of pass transistor circuit with logic '0' and '1' transfer. 6 + 2 + 6

6. Implement the function through dynamic CMOS logic, domino CMOS logic, pass transistor and enhancement load logic :

   $P = (AB + CD) . (A + B)$

   $Q = (P + C) . E.$ 3 + 4 + 3 + 4

7. a) Describe the mechanism of MOS under external bias.

   b) Calculate the zero bias threshold voltage for an NMOS silicon gate transistor that has well doping $N_A = 3 * 10^{17}\ cm^3$, Gate doping $N_D = 10^{20}/cm^3$, Gate oxide thickness 22 Å and $2 * 10^{10}/cm^2$ singly charged positive ions per unit area at the oxide silicon interface. Assume $\varepsilon_{ox} = 4 * \varepsilon_0$.

   c) To cascade two domino logic circuit what type of problems arise and how can these be recovered ?

3 + 5 + 6

8. Write short note on the following : 7 × 2 = 14

   a) DRAM cell

   b) Full adder using half adder through NORA logic.