Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech/SEM-2/PGMVD-201/2012

2012

ANALOG VLSI CIRCUIT & SYSTEMS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *four* from **Group - A** and any *one* from **Group - B**

GROUP – A

Answer any *four* of the following. 4 × 14 = 56

1. a) What is the basic difference between 'Analysis' and 'Synthesis' of an analog VLSI design ? 2

   b) Discuss the analog VLSI design cycle with necessary flow diagram. Explain each step. 2 + 4

   c) How can the passive element 'capacitor' be integrated in an analog VLSI circuit ? Describe with suitable diagrams. 2 + 2 + 2

2. a) What is a MOS switch ? Draw its equivalent circuit and explain the different circuit elements present. Describe the working of a MOS switch. 1 + 2 + 2

b) How can you implement an active, non-linear resistor with the help of a MOS ? Why is it called a MOS diode ? Draw the equivalent circuit and find the effective resistance it offers. 2 + 1 + 2

c) Draw the circuit of a current mirror using two MOSFETs M_1 and M_2. Hence find the ratio-error in the current mirror circuit if $W_1 = 5 \pm 0{\cdot}005$ μm and $W_2 = 20 \pm 0{\cdot}005$ μm. Assume lengths are identical $(L_1 = L_2)$. How can it be corrected using proper layout techniques ? What is the utility of the current mirror ? 1 + 2 + 1

3. a) What are the different types of amplifiers that form the sub-circuits of analog VLSI circuit ? Discuss their relative merits and demerits. 2 + 4

b) Explain the working of an active load inverter with necessary circuit diagram. Find its small signal gain and output resistance. Draw the necessary small signal equivalent circuits. What is the output capacitance for small signal response ? 2 + 1 + 2 + 2 + 1

4. a) What is a differential amplifier ? What is the expression for the output voltage v_0 of a Diff-Amp with two inputs having voltage v_1 and v_2 applied to the two terminals ? What are CMRR and ICMR ? 2 + 2 + 2

b) Explain the working of a CMOS differential amplifier with a suitable diagram and hence find its transconductance. 3 + 1 + 2

c) What is Slew Rate and how can it be improved by proper designing ? 2

5. a) What is a Cascade amplifier ? How does it differ from a Cascade amplifier ? What are the advantages of the Cascade amplifier in comparison to the Inverting amplifier ? 2 + 2 + 2

   b) What is Miller effect ? How does it arise in case of the Cascade amplifier ? Explain in connection with a two stage Cascade amplifier. Give necessary equivalent circuit. 2 + 2 + 2

   c) What are the negative effects of the Miller capacitance ? 2

6. a) What is a current amplifier ? How does it differ from a voltage amplifier ? 2 + 2

   b) Design a Class *A* amplifier for an analog VLSI chip. Calculate the output resistance and the small signal current gain. 2 + 2

   c) What is the difference between an unbuffered and a buffered OP-AMP ? 2

   d) Draw the different stages of a buffered OP-AMP and discuss their significance. 4

GROUP – B

Answer any *one* question. 14 × 1 = 14

7. The channel length of a MOSFET is $L = 1$ μ. Which MOSFET model is best suited for this typical MOSFET ? Give reason for your answer. Name five important parameters used in the model to describe the characteristic equations. What is referred to as the "gradual channel approximation" ? Is this approximation valid for the chosen model ? Give the expressions for the saturation drain current and drain voltage for this model. How this model be modified when the channel length modulation is included ?

   1 + 2 + 2 + 2 + 1 + 2 + 2 + 2

8. a) What are the limitations of SPICE level 3 MOSFET model ? How does BSIM model overcome these limitations ? What important effects are addressed in the BSIM v-3 model ? 2 + 1 + 3

b) The MOSFET MF1 is operated with the substrate shorted to the source, *i.e.* V_{BS} = 0V. The channel length and width of this device is given by L = 5 µm and w = 20 µm. Calculate $V_{D\,sat}$ and $I_{D\,sat}$ obtained in SPICE level 1, Level 2 and Level 3 models for V_{GS} = 5V. Assume μ_n = 800 cm^2/V.S. and for MF1, V_{th} = 0.84V, γ = 1·683, ϕ_B = 0·35 V, $C_{ox} = 3{\cdot}45 \times 10^{-8}$ F/cm^2 and V_{FB} = – 1·27 V.

2 + 3 + 3