Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(IT)ME(CSE)/SEM-1/PGCSE-103/PGIT-103/2011-12

2011

PROCESSOR ARCHITECTURE & ORGANIZATION

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *five* from the rest.

1. A CPU is to be designed with the following specifications :

   (i) All the instructions are of same length and instructions and data reside in the same memory and number of instructions = 32. (ii) Direct memory addressing capability is 2K × 16 bits. (iii) Number of General Purpose Registers including accumulators is 32. (iv) Type of the instructions : (p) Data Transfer (q) Arithmetic and Logical (r) Transfer of Control including CALL instruction (s) Stack operations (t) Machine control. (v) Addressing modes : (p) Direct (q) Immediate (r) Indirect (s) Register.

   You select your own instruction set so that the above specifications are satisfied.

   a) Show the instruction format. 1

   b) What are the sizes of program counter, stack pointer, accumulator and the general purpose registers ? 2

c) Give the block diagram of the Processor and show all the control signals. 4 + 2

d) Write the micro-operations for the fetch cycle and also for the following instructions :

i) CALL < address >

ii) JUMP on condition < address >

iii) ADD < address >

iv) RETURN. 2 × 3

e) Write the Boolean expression for a control signal in the PC which allows the data to go into the PC. 2

f) Using your instructions write a program which will ADD two arrays and store the results in the memory. 3

2. a) Give the logic diagram and CMOS diagram of a basic memory cell. 1 + 2

b) Design a Static memory of size 16 × 4 bit and the data bus is bidirectional. Show the details of block diagram and the selection logic. 5

c) Give the circuit diagram of a basic cell of Dynamic Memory. 2

3. a) Design a 4 Mbyte memory system using 512 kbytes of RAM. Clearly show the block diagram and the necessary control signals. How many modules would be needed ? 2 + 1

   b) What is the need of a chip select line in memory ? 3

   c) Explain how access speed can be enhanced by using low order address interleaving. 4

4. a) What do you mean by pipelining ? What are the advantages of a pipelined CPU ? What is data dependency problem in a pipelined processor ? Explain with an example. Prove that in a pipelined hardware unit if the number of stages is 'K' then the throughput gain will be 'K' times. 2 + 2 + 2

   b) What is Harvard Architecture ? What is the need of it ? 2

   c) With a diagram explain the operation of dynamic pipelining. 2

5. a) What is the basic philosophy behind the RISC architecture ? Give the salient features of the RISC Processor. 2 + 4

   b) Give the block diagram of the internal architecture of a RISC Processor. 4

6. a) What are the characteristics of an SIMD machine ? 2

   b) What is the computational complexity for computing two N × N matrices using an SIMD machine having N processing elements ? 2

c) An SIMD having 8 PEs are connected through a dynamic n cube interconnection network. Determine the control matrix for connecting PE (i) to PE ($i + 3$). 3

d) Give the structure of a PE of an SIMD machine. 3

7. a) What is 'Reconfigurable Computing' ? Why can FPGA be used as a key element for developing a "Reconfigurable Computing System" ? Show the architecture of an FPGA and indicate its basic blocks. 2 + 1

b) Giving a circuit diagram, show how an FPGA can be configured from the bit-stream stored in Flash Memory. 4

c) Show the steps involved in FPGA Design Flow. 3

8. a) What are the characteristics of a "systolic processor" ? 2

b) Give the architecture of a "systolic processor" to compute the following : 3

$$y(n) = x(n-k).h(k) \text{ for } k = 0 \text{ to } N-1$$

Assume that $x(n)$ is the input and $y(n)$ is the output for nth sequence. Input data sequences are arriving at regular interval.

c) Explain the behaviour of the basic systolic cell using a block diagram. 1

d) What are the characteristics of a Vector Processor ? 2

e) What is VLIW architecture ? What is its advantage ? 2