



Name : .....  
Roll No. : .....  
Invigilator's Signature : .....

**CS/M. TECH (ECE-COMM)/SEM-2/MCE-204C/2012**

**2012**

**INTEGRABLE CIRCUITS & DESIGN**

*Time Allotted : 3 Hours*

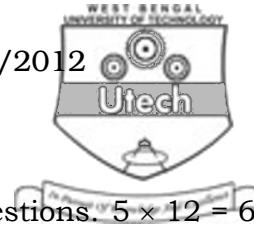
*Full Marks : 70*

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP – A**

1. Answer any *five* from the following questions :  $5 \times 2 = 10$ 
  - a) What are four generations of integrated circuits ?
  - b) Define the static resistance and the dynamic resistance of *p-n* diode.
  - c) Implement an XOR gate using CMOS transmission gate.
  - d) What is precharge-evaluate logic ?
  - e) What are the main constructional differences between an MOSFET and a BJT ?
  - f) What is the mass action law for the carrier concentrations in a semiconductor ? What is its significance ?
  - g) What is the advantage of differential operation over single-ended signaling ?



**GROUP – B**

Answer any *five* of the following questions.  $5 \times 12 = 60$

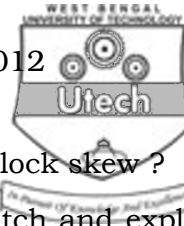
2. a) What do you mean by channel length modulation ? How is drain current related with channel length modulation coefficient ? 2 + 2
- b) The reverse saturation current at 300K of a p-n junction Ge diode is  $5\mu\text{A}$ . Find the voltage to be applied across the junction to obtain a forward current of 50mA. Given non-ideality factor  $\eta = 1$ , Boltzmann's constant  $k = 1.38 \times 10^{-23} \text{ J/K}$ , electron charge  $q = 1.6 \times 10^{-19} \text{ C}$ . 4
- c) Consider an  $n$ -channel MOSFET with  $t_{\text{ox}} = 20\text{nm}$ ,  $\mu_n = 650 \text{ cm}^2/\text{V-s}$ ,  $V_{\text{th}} = 0.8\text{V}$  and  $W/L = 10$ . Find the drain current in the following cases :
  - i)  $V_{\text{GS}} = 5 \text{ V}$  and  $V_{\text{DS}} = 1\text{V}$
  - ii)  $V_{\text{GS}} = 2 \text{ V}$  and  $V_{\text{DS}} = 1.2\text{V}$  4
3. a) Draw the circuit diagram of CMOS inverter and explain its operation using VTC curve. 2
- b) Consider a resistive load inverter circuit with  $V_{\text{DD}} = 5 \text{ V}$ ,  $K_{n'} = 20\mu\text{A}/\text{V}^2$ ,  $V_{\text{TO}} = 0.8\text{V}$ ,  $R_L = 200 \text{ k}\Omega$  and  $W/L = 2$ . Calculate the critical voltages ( $V_{\text{IL}}$ ,  $V_{\text{OL}}$ ,  $V_{\text{IH}}$ ,  $V_{\text{OH}}$ ) on the VTC and find the noise margins of the circuit. 5



- c) Derive the expression for inverter threshold voltage for CMOS inverter :

$$V_{thINV} = \frac{VT_{on} + \sqrt{\frac{k_p}{k_n}} (V_{DD} + VT_{OP})}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)} \quad 5$$

4. a) What do you mean by "Mosfet in weak inversion" ? Write down the drain current equation for MOSFET in weak inversion. 1 + 2
- b) Design a 4 : 1 multiplexer circuit using TG switches. 4
- c) Why dynamic logic can't be cascaded directly ? Implement the Boolean function  $F = (ABC + DE)'$  using dynamic CMOS logic. 2 + 3
5. a) A CMOS inverter has a power supply voltage  $V_{DD} = 5V$ . Using average current method calculate the fall time  $t_{fall}$ .  $V_{out} = V_{90\%} = 4.5V$  and  $V_{out} = V_{10\%} = 5V$ . The output load capacitance is 1pF. The nMOS transistor parameter is given as :  $\mu_n C_{ox} = 20\mu A/V^2$ ,  $(W/L)_n = 10$ ,  $V_{Tn} = 1.0V$ . 3
- b) Design a static CMOS logic to implement the Boolean function  $F = AB + AB' C + A' C'$ . 4
- c) Draw the layout and schematic diagram of 2-input static CMOS NOR gate and identify the corresponding components in the two drawings. 5



6. a) What are the problems associated with clock skew ? 3  
b) Design a NOR2 gate based CMOS SR latch and explain its operation. 4  
c) Design a Full adder circuit using CMOS logic. 5
7. a) Draw the small signal equivalent circuit model of MOSFET and find output resistance. 3  
b) With circuit diagram, explain the operation of MOS current mirror. 4  
c) Derive the small signal voltage gain for common gate amplifier and compare it with common source stage amplifier. 5
8. Write short notes on any *two* of the following : 6 + 6  
a) Cascoding stage  
b) CMOS differential amplifier  
c) Domino Logic  
d) Switched capacitor circuits.
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