Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M. TECH (ECE-COMM)/SEM-2/MCE-204C/2012

2012
INTEGRABLE CIRCUITS & DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

1. Answer any *five* from the following questions : 5 × 2 = 10

   a) What are four generations of integrated circuits ?

   b) Define the static resistance and the dynamic resistance of *p-n* diode.

   c) Implement an XOR gate using CMOS transmission gate.

   d) What is precharge-evaluate logic ?

   e) What are the main constructional differences between an MOSFET and a BJT ?

   f) What is the mass action law for the carrier concentrations in a semiconductor ? What is its significance ?

   g) What is the advantage of differential operation over single-ended signaling ?

GROUP – B

Answer any *five* of the following questions. $5 \times 12 = 60$

2. a) What do you mean by channel length modulation ? How is drain current related with channel length modulation coefficient ? 2 + 2

b) The reverse saturation current at 300K of a p-n junction Ge diode is 5μA. Find the voltage to be applied across the junction to obtain a forward current of 50mA. Given non-ideality factor $\eta = 1$, Boltzmann's constant $k = 1{\cdot}38 \times 10^{-23}$ J/K, electron charge $q = 1{\cdot}6 \times 10^{-9}$ C. 4

c) Consider an *n*-channel MOSFET with $t_{ox} = 20$nm, $\mu_n = 650\ cm^2$/V-s, $V_{th} = 0{\cdot}8$V and W/L = 10. Find the drain current in the following cases :

i) $V_{GS} = 5$ V and $V_{DS} = 1$V

ii) $V_{GS} = 2$ V and $V_{DS} = 1{\cdot}2$V 4

3. a) Draw the circuit diagram of CMOS inverter and explain its operation using VTC curve. 2

b) Consider a resistive load inverter circuit with $V_{DD} = 5$ V, $K_{n'} = 20\mu A/V^2$, $V_{TO} = 0{\cdot}8$V, RL = 200 kΩ and W/L = 2. Calculate the critical voltages (V_{IL}, V_{OL}, V_{IH}, V_{OH}) on the VTC and find the noise margins of the circuit. 5

c) Derive the expression for inverter threshold voltage for CMOS inverter :

$$V_{th\,INV} = \frac{VTon + \sqrt{\frac{k_p}{k_n}}\,(V_{DD} + VT_{OP})}{\left(1 + \sqrt{\frac{k_p}{k_n}}\right)}$$ 5

4. a) What do you mean by "Mosfet in weak inversion" ? Write down the drain current equation for MOSFET in weak inversion. 1 + 2

b) Design a 4 : 1 multiplexer circuit using TG switches. 4

c) Why dynamic logic can't be cascaded directly ? Implement the Boolean function F = (ABC + DE)' using dynamic CMOS logic. 2 + 3

5. a) A CMOS inverter has a power supply voltage V_{DD} = 5 V. Using average current method calculate the fall time i fall. V_{out} = V90% = 4·5V and V_{out} = V10% = 5V. The output load capacitance is 1pF. The nMOS transistor parameter is given as : μnCox = 20μA/V^2, (W/L) n = 10, VT, n = 1·0V. 3

b) Design a static CMOS logic to implement the Boolean fuction $F = AB + AB^{/} C + A^{/} C^{/}$. 4

c) Draw the layout and schematic diagram of 2-input static CMOS NOR gate and identity the corresponding components in the two drawings. 5

6. a) What are the problems associated with clock skew ? 3

   b) Design a NOR2 gate based CMOS SR latch and explain its operation. 4

   c) Design a Full adder circuit using CMOS logic. 5

7. a) Draw the small signal equivalent circuit model of MOSFET and find output resistance. 3

   b) With circuit diagram, explain the operation of MOS current mirror. 4

   c) Derive the small signal voltage gain for common gate amplifier and compare it with common source stage amplifier. 5

8. Write short notes on any *two* of the following : 6 + 6

   a) Cascoding stage

   b) CMOS differential amplifier

   c) Domino Logic

   d) Switched capacitor circuits.