*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/M.TECH(ECE)/SEM-3/MVLSI-302/2012-13**

**2012**

# ADVANCED ANALOG & DIGITAL VLSI CIRCUIT & SYSTEMS

*Time Allotted* : 3 Hours *Full Marks* : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

*The mathematical symbols used in the questions are standard.*

## GROUP – A

## ( Objective Type Questions )

1. Answer any *five* of the following : $5 \times 2 = 10$

   i) The odd number of inverters forms a close loop with positive feedback in a ring oscillator. Calculate the frequency of oscillation.

   ii) If $K_n = 3K_p$, what is the ratio of $(W/L)_p$ and $(W/L)_n$ to make $\beta_n = \beta_p$ ?

   iii) Find $n$ input NAND gate driving a capacitance load $C_L$, what is the approximate expression of rising and falling propagation delay ?

iv) What is the minimum threshold voltage for which the leakage current through an off transistor ($V_{gs} = 0$) is $10^3$ times less than that of a transistor that is barely on ($V_{gs} = V_{th}$) at room temperature, if $n$ = 1·5 ?

v) If we apply a voltage $V_g$ at the gate of a $n$-MOS and 1 V at the source with drain terminal opened, plot the on-resistance of $n$-MOS as a function of $V_g$. Assume $\mu_n C_{ox} = 50\,\mu A/V^2$, $(W/L)_n = 10$ and $V_{TH} = 0 \cdot 7$ V.

vi) Explain with an example the caveat of Miller's theorem.

vii) What do you mean by wiring/routing track in stick diagram ? If one wire has a width of 4λ and a spacing of 4λ to the next wire, then find the track pitch.

viii) What is the use of delay statement in Verilog ? Write a simple Verilog example defining an inverter with a 40 unit of propagation delay.

## GROUP – B

## ( Short Answer Type Questions )

Answer any *three* of the following $3 \times 5 = 15$

2. Explain the reduction and concatenation operators in Verilog.
3. What are the different data types in Verilog ? Explain the net data type of wire. 2 + 3
4. What is logical effort ? Deduce the relation between normalized delay ( $d$ ), logical effort ( $f$ ), electrical effort ( $h$ ) and parasitic delay ( $p$ ).

5. Write all the three equations of a MOS $g_m$ and plot the graphs showing $g_m$ as a function of overdrive voltage, drain current and $W/L$ ratio.
6. Explain the following terms with examples :
   i) Stuck-at fault
   ii) Bridging fault. 3 + 2
7. What are fault equivalence and fault dominance in logic gates ? 2 + 3

## GROUP – C

### ( Long Answer Type Questions )

Answer any *three* of the following. 3 × 15 = 45

8. a) Calculate the output voltage swing limits (for $V_{dd}$ = 5 V), small signal *dc* gain, the output resistance and the –3dB frequency of a CS amplifier with current source load in figure 1a if $(W/L)_1 = 2\,\mu m$, $(W/L)_2 = 1\,\mu m$, $C_{gd1} = 0 \cdot 5\,fF$, $C_{bd1} = C_{bd2} = 10fF$, $C_L = 1\,pf$, and $I_{d1} = I_{d2} = 100\,\mu A$, $V_{T0n} = 0 \cdot 7\,V$, $V_{T0p} = -0 \cdot 7\,V$, $K_n = 110\,\mu A/V^2$, $K_p = 50\,\mu A/V^2$, $\gamma = 0 \cdot 4V^{1/2}$ for NMOS, $\gamma = 0 \cdot 574V^{1/2}$ for *p*-MOS, $\lambda = 0 \cdot 04\,V^{-1}$ for *p*-MOS and $\lambda = 0 \cdot 05\,V^{-1}$ for *n*-MOS. What is the value of $V_{GB}$ to make $I_{d1} = I_{d2} = 291\ \mu A$ ?

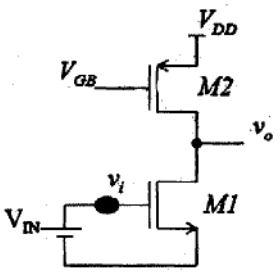


Fig. 1a

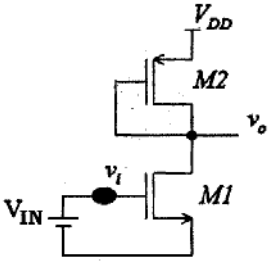


Fig. 1b

b) Figures 1c and 1d indicate the plots of current versus voltage of an *n*-MOS CS stage with diode connected load. Indicate the operating conditions of the two *n*-MOSs ($M_1$ : Driver and $M_2$ : Load) used in this configuration in the three regions marked I, II and III in figure 1c and 1d. State with justification the operating region.

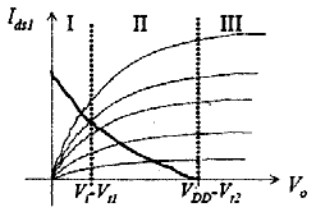


Fig. 1c

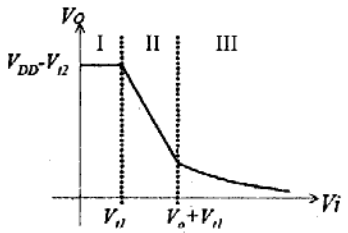


Fig. 1d

c) Design a 4 : 1 MUX using component instantiation in Verilog where the basic building block is a tri-state buffer. 6 + 4 + 5

9. a) Using the material and device parameters in Q.No.8(a), design a two-state Op-Amp as shown in Fig. 2 that meets the following specifications :

$A_v(0) > 5000$, $V_{DD} = 2 \cdot 5\,\text{V}$, $V_{SS} = -2 \cdot 5\,\text{V}$,

GBW = 10 MHz, $C_L = 2\,\text{pF}, SR \geq 10\ \text{V}/\mu\text{s}$,

$V_{OUT}$ (peak to peak) $= \pm 2\,\text{V}$, ICMR = –1 V to 2 V,

$P_{diss} \leq 1\text{mW}$, $V_A$ = 20 V.

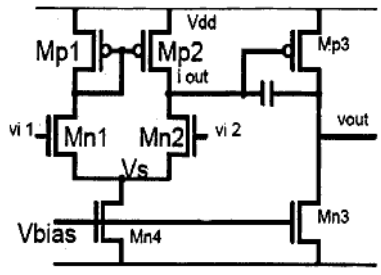


Fig. 2

b) "The slew rate of 2-state Op-Amp is limited by the first stage only." Justify. If 741 Op-Amp has a slew rate of 1V/μs with $V_{OUT}$ (peak to peak) = ± 14 V then what is the maximum operating frequency for undistorted output ? 8 + 4 + 3

10. a) What is blocking and Non-blocking Procedural Assignments in Verilog ? Design a 4-bit right-shift register using blocking and non-blocking approaches of Verilog with always block.

b) Using *D* algorithm determine the suitable test vector of the circuit of Fig.3, if node *B* is at stuck-at-0 fault using *D* algorithm. ( 3 + 4 ) + 8

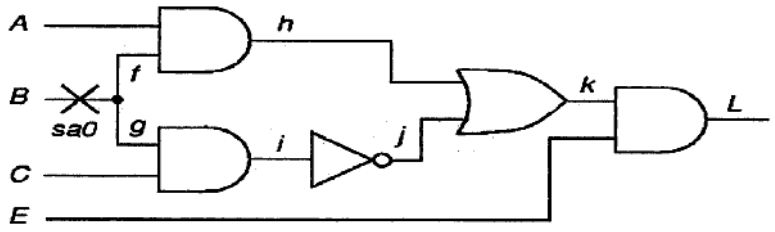


Fig. 3

11. a) Sketch a 2-input NAND gate with the transistor channel width chosen to achieve the effective rise and fall resistance equal to that of an unit inverter. Compute the rising and falling propagation delay (in terms of $R$ and $C$ ) of a NAND gate driving $h$ identical NOR gates. If $C$ = 2 fF/μm and $R$ = 2·5 kΩ. μm then what is the delay of a fan-out of 3 NAND gate ?

    b) What is the logical effort of 2-input XOR gate and 3-input NAND gate ?

    c) Explain the different Fault Table analyses of AND, OR and NOR gates. ( 2 + 3 + 2 ) + 2 + 6

12. a) Write down the Verilog code of a 4-bit binary up counter and its test bench counterpart.

    b) Estimate the minimum delay of the path from $A$ to $B$ in the Fig. 4. Choose transistor sizes to achieve this delay. The initial NAND2 gate presents a load of 8λ of the transistor channel width and the output load is equivalent to 45λ of the transistor channel width. 8 + 7

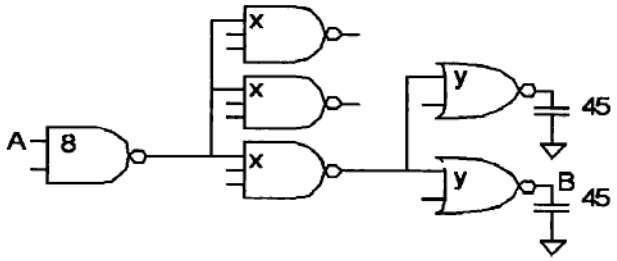


Fig. 4

13. a) Briefly explain the construction of ROBDD in connection with logic synthesis.

b) Construct ROBDD of the following Boolean functions, given in SOP form :

(i) $f_1 = ab' + a'b$, (ii) $f_2 = abc + b'd + c'd$.

c) What is state encoding ? Discuss the different state encoding techniques. 4 + ( 3 + 4 ) + ( 1 + 3 )

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