

Name :

Roll No. :

Invigilator's Signature :

**CS/M.TECH (ECE)/SEM-2/MVLSI-201/2013
2013**

PROCESSOR ARCHITECTURE FOR VLSI

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

GROUP – A

(Short Answer Type Questions)

Answer *all* of the following questions.

1. Answer the following questions :

- a) What is Flag register ? 2
- b) Distinguish between Von-Neumann and Harvard architecture. 2
- c) What are the operation of latch input and output enable of register ? 2
- d) What is pipelining ? Compare between sequential execution and pipeline execution architecture. 3



- e) For a given number of stages of the processor, a number of tasks and period of synchronizing clock, find the speedup, throughput and efficiency of the pipelined processor. 2
- f) Comment on the impact of branch instructions in pipelined architecture. Show with an example, how to avoid or deal with conditional and unconditional branch instruction. 3

GROUP - B

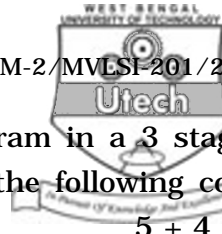
(Long Answer Type Questions)

Answer any *four* of the following questions.

2. Compare between parallel architecture and multi-core architecture. Discuss Nehalems Architecture. State Amdhal's Law. Discuss the demerits of Amdhal's Law. State Gustafson's Law. Discuss how it overcomes the demerits of Amdhal's Law. Compare between Shared memory multicore, Distributed memory multicore and Manycore architectures.

2 + 2 + 4 + 4 + 2

3. a) What are the different pipeline hazards ? How do you avoid them ?
- b) A linear instruction pipeline having ten stages operates at 25 MHz. If one instruction is issued per clock cycle, what will be the speedup factor to execute a program of 15000 instruction as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay ? Ignore penalties due to branch instructions and out of sequence execution.



- c) Compare using timing sequence diagram in a 3 stages pipeline and in a 5 stages pipeline, the following code segment :

```

MOV R1, 0F h      [ R1 = 0F h ]
MOV R2, 05 h      [ R2 = 05 h ]
LDA 10 h          [ ACC = 10 h ]
ADD ACC, R1, ACC  [ ACC = R1 + ACC ]
SUB Acc, R2, ACC  [ ACC = R2 - ACC ]
STA R3            [ R3 = ACC ]
    
```

4. What do you mean by SOC (system on chip) ? Give brief description of three platform based SOC architecture.

4 + 10

5. What is the basic architectural and functional difference between Digital Signal Processor and General Purpose Processor ? Why we prefer Digital Signal Processor in signal Processing Field ? With appropriate example, discuss about evolution of Digital Signal Processor.

6 + 4 + 4

6. Explain that UMA, NUMA and COMA architectural models for a multiprocessor system. Explain briefly Cache Coherence problem related to COMA model and the different methods to cope the problem.

10 + 4

7. Explain briefly RAW architecture with neat diagram. Describe with neat diagram of TMS320C6XXX series processor architecture.

6 + 8

=====