Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH (ECE-VLSI)/SEM-2/MVLSI-201/2012

2012

PROCESS ARCHITECTURE FOR VLSI

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Objective Type Questions)

1. Answer very briefly : 10 × 1 = 10

   i) Compare Hard-macro & Soft-macro in connection with embedded system design.

   ii) Compare Von-Neumann and Harvard Architecture of a processor based system.

   iii) Most instructions in ARM Microcontroller are RISCy. Explain.

   iv) Explain why supporting binary compatibility is problematic for VLIWs.

   v) What are the essential building blocks for a System On Chip (SOC) implementation in a generic form ?

vi) What is Pipelining in a processor ?

vii) Illustrate CMOS power optimization techniques used to design Embedded Processors.

viii) Power Measurement resources are included in the ARM Core used in OMAP of a mobile hand set, whereas the same Power Measurement resources are not included in the ARM processor used in the GPS receivers. Explain in detail with reasons.

ix) Highlight IEEE Standard Single Precision Floating Point Format.

x) What do you mean by Ericsson-VLSI Bluetooth Baseband Controller ?

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Implement a hardware for one cycle Multiply-Accumulate Instruction often used in a DSP processor. Also design a Pipelined MAC Data path.

3. Explain the functions of TDM Serial Port and MAC Unit in the DSP.

4. Illustrate *Q* 15/16 representation of binary numbers for computation in DSP Processors.

5. What is need for Exponent Encoder to compute an exponent value of a 40-bit Data item in TMS320C5X family of DSPs ?

6. CISC Processors have better code density than the RISC processors. Explain in a bit detail with reasons.

7. Explain Super Scalar Architecture with illustration and block schematic representation. Does ARM Support Super Scalar Architecture ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

8. Explain briefly the architecture of ARM processor with a block schematic representation. Also briefly highlight the features for which this processor is directly used as an integrated IP Core in the Mobile Communication segment compared to any other Embedded Processors.

9. What is Pipeline hazards ? Elaborate your concept with reference to (i) Pipelined instruction execution, (ii) Pipe-lined read-after-write and (iii) Pipelined branch behaviour.

10. Explain briefly the architecture of IBM Power PC processor with a block schematic representation.

11. Suggest the Architecture Design of a Simple Processor MU0 as used in the University of Manchester Processor Design Program. This conceptual RISC Processor should have a Program Counter (PC) register, an Accumulator (ACC) register, an Instruction Register (IR) and an Arithmetic Logic Unit (ALU). MU0 is a 16 bit machine with a 12-bit address space. Each location is organised as a 16-bit location. MU0 Instruction Set supports only 8 instructions with 4-bit Opcode. Instructions supported are LDA S, STO S, ADD S, SUB S, JMP S, JGE S, JNE S and STP. Show the MU0 Logic Design and Data Path Design.

12. Write short notes on any *three* of the following : 3 × 5

a) Architecture of Configurable Logic Block (CLB)

b) Code Density of Thumb Architecture of ARM Processor

c) Boot Loader

d) On chip peripherals of TMS320C50 DSP

e) Direct Memory Access (DMA) Controller of DSP

f) Single Access RAM (SARAM).