Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M. Tech (ECE)/SEM-2/MCE-204-C/2013

2013

INTEGRATABLE CIRCUITS AND DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

Answer question no. 1 and any *four* from the rest.

1. Answer the following questions : $7 \times 2 = 14$

   i) What is pull down device ? Justify your answer.

      a) PMOS b) NMOS

      c) CMOS d) BJT

   ii) Which of the following processing techniques would be used to create the source and drain regions of a transistor ? Briefly describe the process.

      a) Oxidation

      b) Ion implantation

      c) Sputtering

      d) Polysilicon deposition.

iii) Si is preferred over Ge because
   a) Si is cheaper
   b) Si band gap is large
   c) Si technology is matched
   d) All of these.

iv) Which of the following has minimum propagation delay ?
   a) ECL b) TTL
   c) RTL d) DTL.

v) Which of the following is/are advantage(s) of CMOS ?
   a) Wide range of supply voltage
   b) Greater noise margin
   c) Large packaging density
   d) All of these.

vi) The ON-resistance of a MOSFET
   a) linearly increases with Vgs
   b) linearly decrease with Vgs
   c) exponentially increases with Vgs
   d) non-linearly decreases with Vgs.

vii) State True/False
   a) Switching speed of MOS Op-Amp is higher than Bipolar Op-AMP.
   b) Source followers is used for voltage amplifier
   c) Slew rate increase speed of response increase
   d) Temperature is less effective when biasing is used
   e) PSRR is very high in op-amp.

2. What is oxidation ? What are the different types of oxidation used in IC Fabrication ? What is the function of photo-resist in fabrication process ? What is the difference between negative and positive photo-resist ? 3 + 4 + 4 + 3

3. What is meant by "Epitaxy" ? Describe Homo-Epitaxy. Why is NAND gate preferred over NOR gate for fabrication ? Why is the substrate in NMOS connected to Ground and in PMOS to VDD ? 2 + 2 + 5 + 5

4. In CMOS technolgoy, in digital design, why do we design the size of PMOS to be higher than the NMOS ? What determines the size of PMOS with respect to NMOS ? What is the current mirror ? Explain it along with diagram. 5 + 3 + 3 + 3

5. What are the four generations of integrated circuits ? Discuss the advantages and disadvantages of IC. What do you mean by subthreshold conduction ? How does it effect the design an IC ? 3 + 4 + 4 + 3

6. What are the disadvantages of CMOS inverter ? What happens when the PMOS and NMOS are interchanged with one another in an inverter ? Locate five distinct regions for CMOS inverter and specify the operating modes of the MOSFET on those regions of the VTC. 3 + 2 + 5 + 4

7. Describe how CMOS works as switch. Implement F = AB + AC + BC. Explain how MOSFET behaves as a capacitor. Explain floating MOS capacitor. 5 + 3 + 2 + 4