Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE-VLSI)/SEM-2/MVLSI-203/2011

2011

ANALOG IC DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Objective Type Questions)

1. Answer any *seven* of the following : 7 × 2 = 14

   a) What is floating active resistor ?

   b) What is the limitation of NMOS switch ?

   c) What are the advantages of push-pull inverter over current source inverter ?

   d) What is integral non-linearity of a DAC ?

   e) Draw the negative switch capacitor transresistance equivalent circuit.

   f) What is phase noise of an oscillator ?

   g) What are lock range & capture range of a PLL ?

   h) What is ICMR & CMRR ?

   i) Why CMOS circuits consume less power ?

   j) What are the advantages of folded cascode OP-AMP ?

GROUP – B

(Long Answer Type Questions)

Answer any *four* of the following. 4 × 14 = 56

2. a) How can a MOS transistor be used as a switch ? Find out the small signal channel resistance of a MOS transistor acting as a switch.

   b) What are the differences between current sink & current source ? Draw & explain operating principle of a standard cascode current sink.

   c) What are the effects that cause the current mirror to be different from ideal situation ? What is source follower ? (3 + 2) + (2 + 3) + (2 + 2)

3. a) Draw & explain operating principle of a CMOS differential amplifier using current mirror load. Find out the noise model of the same.

   b) Explain with suitable diagram the large singal characteristics of a simple cascode amplifier. Draw its voltage transfer characteristics.

   c) What is a current amplifier ? (3 + 2) + (5 + 2) + 2

4. a) Define the following terms in connection with DAC :

      i) full scale range

      ii) quantization noise

      iii) effective no. of bits. With suitable circuit diagram explain the operation of a charge scaling DAC.

   b) Explain the concept of a multiple bit pipeline ADC.

   (6 + 4) + 4

5. a) Analyze the basic operation of a switch capacitor circuit using two phase non-overlapping clock.

   b) Draw & explain the operation of a first order switch capacitor low pass circuit.

   c) Design a switch capacitor first order circuit that has a low frequency gain of +10 & a – 3dB frequency of 1 kHz. Give the value of capacitor ratios of α_1 & α_2. Use a clock frequency of 100 kHz. 4 + 6 + 4

6. a) What is compensation of Op-Amp ? Discuss Millar compensation of two-stage Op-Amp.

   b) What is micro-power Op-Amp ? Give an explanation of two-stage Millar Op-Amp operating in weak inversion.

   (3 + 4) + 2 + 5

7. a) Find the propagation delay time of an open-loop comparator that has a dominant pole at 10^3 rad/s, a dc gain of 10^4 , a slew rate of lV/μs and a binary output voltage swing of lV. Assume that the applied input voltage is 10mV.

   b) What are different types of open loop comparator ? Explain any one of them.

   c) How can performance of open loop comparator be improved ? 5 + (2 + 3) + 4

8. a) How are monolithic inductors fabricated on the same substrate of an RF circuit ?

   b) What are the design considerations of LNA ?

   c) Draw & explain the operation of a passive CMOS mixer.

   5 + 4 + 5