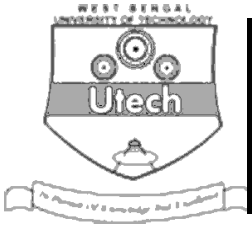
CS/M.TECH (ECE)/SEM-2/EC-1002/09
ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN (SEMESTER - 2)



1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No. | | | | | | | | | | | | | | |

Roll No. of the Candidate | | | | | | | | | | | | | | |

CS/M.TECH (ECE)/SEM-2/EC-1002/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JULY – 2009

ADVANCED ANALOG INTEGRATED CIRCUIT DESIGN (SEMESTER - 2)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. You have to answer the questions in the space provided marked 'Answer Sheet'. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

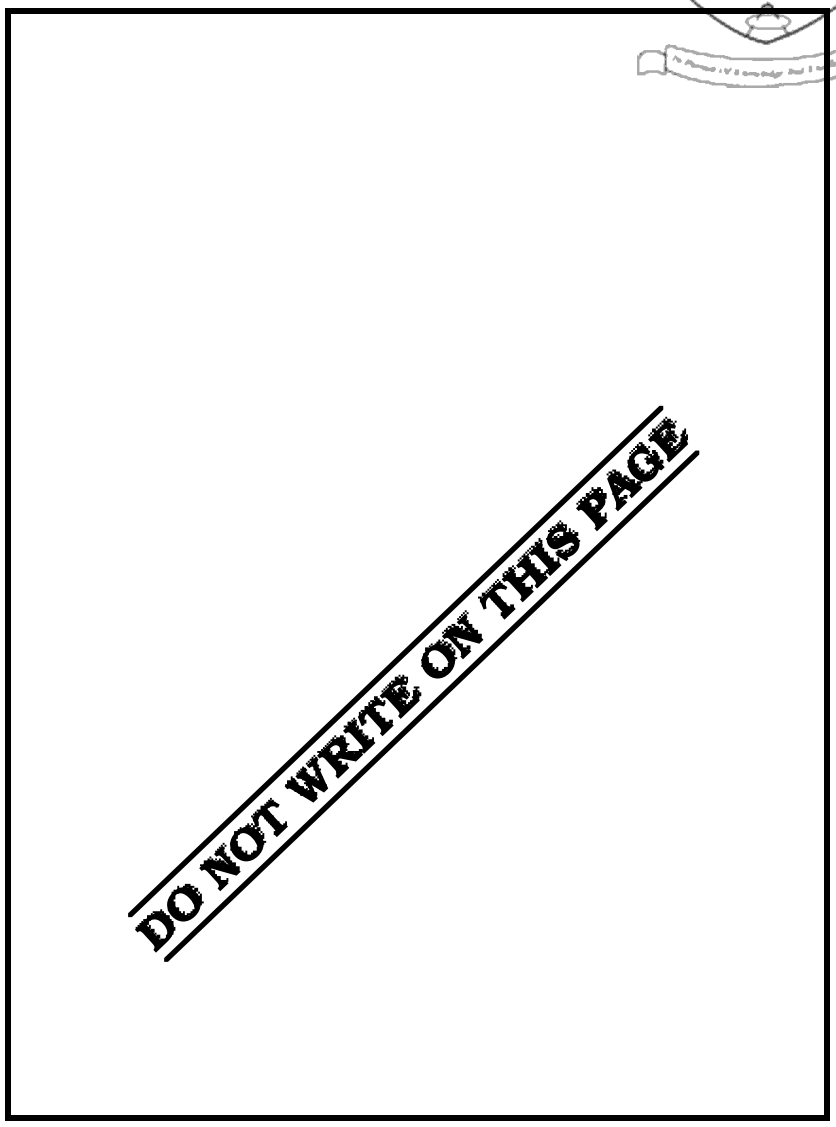
No additional sheets are to be used and no loose paper will be provided

FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

Question Number											***Total Marks***	***Examiner's Signature***
Marks Obtained												

.....
Head-Examiner/Co-Ordinator/Scrutineer



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The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A

Answer Question No. *1* and any *two* from the rest.

1. Write short notes on any *three* of the following : 3 × 5 = 15

   i) Critical field in DSM Technology

   ii) Logical effort

   iii) Elmore Delay

   iv) Stray insensitive switching capacitor realization of a non-inverting integrator

   v) Sizing an inverter.

2. What is meant by velocity saturation in short channel MOS gates and how it affects the pinch-off point, $V_{D,sat}$? Determine the value of $V_{D,sat}$ for an NMOS device assuming V_{GS} = 1·8 V, V_T = 0·5 V and Channel length = 180 nm.

   (Given, critical electric field for electrons, $E_{cn} = 6 \times 10^4$ V/cm) 2 + 4 + 4

3. Design a suitable circuit to implement an 8-input AND gate to drive a capacitor load of 200 fF and with an input capacitance limited to 10 fF with the smallest delay. Justify your steps. 10

4. What is interconnect in VLSI and how it has become so important now ? Show the variation of gate delay and interconnect delay with minimum feature size.

A uniform polysilicon interconnect of length 0·5 mm and width 5 μm is used at a gate output. Estimate the total delay using a lumped RC. 10

Assume : [i) sheet resistance 30Ω/□

ii) unit area capacitance = 0·066 fF/μm ^{2}

iii) unit length capacitance = 0·046 fF/μm]

5. Explain clearly how a switched capacitor can be used to replace a resistance in integrated circuits. Mention its advantages and disadvantages. Design a switched capacitor filter using a high gain Op-Amp with the following frequency response :

i) gain 20 db from 0 to 1 kHz.

ii) gain drops uniformly at 20 db/decade after 1 kHz and becomes 0 db at 10 kHz.

Use a clock of $2\pi \times 100$ kHz and assume the value of the switched capacitor between output and op-amp input terminal = 100 fF. 3 + 2 + 5

GROUP - B

Answer Question No. *6* & any *two* from the rest.

6. Why in case of a single ended differential amplifier one I/P terminal is marked as (–) 2 another one as (+ ve) ? 5

7. What is the block diagram of a CMOS Op-Amp ? Design any 2 stage CMOS Op-Amp.

5 + 10

8. Design cascode current sink circuit and mention its advantages.

If $\Delta k' / k' = \pm 5\%$ & $\Delta V_T / (V_{GS} - V_T) = \pm 10\%$, then what will be the error in current mirror gain ? 8 + 3 + 4

9. Explain with a circuit diagram, the operation of a differential amplifier. What is CMRR ? Determine the CMRR of the foll. circuit. 10 + 5

Dia.

10. Define current source & sink. Show how the O/P resistance of a current sink can be increased.

Explain the operation of a band gap voltage reference source in a VLSI circuit.

5 + 7 + 3

END