*Name* : .....

*Roll No.* : .....

*Invigilator's Signature* : .....

**CS/M.TECH(ECE-VLSI)/SEM-1/MVLSI-102/2011-12**

**2011**

# VLSI DEVICE AND MODELLING

*Time Allotted* : 3 Hours Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

## GROUP – A

**( Objective Type Questions )**

1. What do you mean by sub-threshold conduction ? 2
2. What is hot electron effect in MOSFET and how to minimize this effect ? 3
3. What do you mean by channel length modulation ? 2
4. Define Threshold voltage of MOS device. What are the parameters on which threshold voltage is dependent and how ? 3
5. For equal size ( width ) NMOS and PMOS device, which is faster and why ? 2
6. For a 2-input NAND gate having equal size NMOS transistors, which NMOS has higher threshold voltage and why ? 2

**GROUP – B**

Answer any *four* questions.

7. Why MOSFET is used for VLSI circuits ? For an NMOS device operating in saturation, plot transconductance versus ( VGS + VTH ) if (a) ID constant (b) W/L constant. To design the width of a MOSFET such that a specified current is induced for a given applied bias, consider an ideal *n*-channel MOSFET with parameters L = 1·25 μm, μn = 650 $cm^2$ /V–s,
cox = 6·9 × $10^{-8}$ $F/cm^2$ and $V_T$ = 0·65 V. Design the channel width W such that ID ( sat ) = 4 mA for VGS = 5V.

3 + 6 + 5

8. Explain surface scattering in MOSFET. How is it dependent on gate voltage ? Describe short channel effect ( SCE ). How halo doping can minimize SCE in MOSFET ? How to minimize scattering in the MOSFET by changing external and internal parameters ? 4 + 2 + 3 + 5

9. What do you mean by Ballistic Transport ? Draw the schematic cross-section of *n* MOS capacitor and energy band diagram under different bias conditions. Explain 2DEG formation in MOSFET. Compare 2DEG in heterojunction and MOSFET. 2 + 5 + 3 + 4

10. a) Draw Transfer Curve for a CMOS inverter ( $V_{out}$ $vs$ $V_{in}$ Plot ).

b) Show different regions of Transfer Curve and specify NMOS and PMOS conduction state for each region of Transfer Curve.

c) Specify equivalent circuit model of CMOS inverter for each region of Transfer Curve.

d) If width of PMOS ( $W_p$ ) grows with respect to NMOS width ( $W_n$ ), how does CMOS inverter Transfer Curve change ? 2 + 5 + 3 + 4

11. a) What are the components of Total Capacitive load ( $C_{total}$ ) of a CMOS driver considering that driver gate is inverter and receiving gate is also inverter ?

b) What are the parameters on which CMOS gate delay depends and how ?

c) What are key components of CMOS gate power ?

d) What are the sources of CMOS noise and what is Noise margin ? 4 + 3 + 3 + 4

12. a) What is stage ratio for chain of CMOS gates for minimum delay through the chain and why ?

b) For a 3 Input NAND gate, if one of the PMOS transistor width ( $W_p$ ) is 2 μm, what should be the width of other NMOS and PMOS transistors for equal rise and fall delay ? Assume Electron Mobility is 2 times Hole Mobility.

c) For a 4 Input NOR gate, if one of the NMOS transistor width ( $W_n$ ) is 3 μm, what should be the width of other NMOS and PMOS transistors for equal rise and fall delay ? Assume Electron Mobility is 2 times Hole Mobility.

d) What is the definition of constant field scaling of MOS Transistor ? How does this scaling change MOS transistor device and circuit paramenters ?

4 + 3 + 3 + 4