Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (ECE)/SEM-1/MVLSI-105B/2011-12

2011

EMBEDDED SYSTEM FUNDAMENTALS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Objective Type Questions)

1. State whether the statements are *True* or *False*. Justify with proper reasons for any *five* of the following : 5 × 2 = 10

   i) An architecture used in any microcontroller is Princepton architecture.

   ii) ASSP chip has a large number of arrays with each element having feasible links.

   iii) OTP ROM has highest storage performance.

   iv) 8051 is a 16-bit microprocessor.

   v) Compiler is a program that combines object code files into an executable program.

   vi) Mainframe is not an Embedded system.

   vii) NV RAM is a volatile memory.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Given a 1-level cache design where the hit rates are given with following specifications.

   i) Cache access time of 50 nsec.

   ii) Main memory access time of 500 nsec.

   iii) 80% of memory requests are for read.

   iv) Hit ratio of 0·9 for read access and write through scheme is used.

   Calculate the following :

   a) Average access time of the memory system considering only memory read cycle.

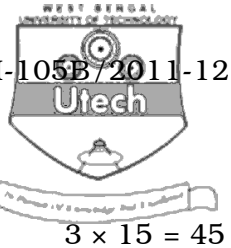
   b) Average access time of the system both for read and write requests.

3. There is a (512 × 8) ROM and 4 RAMs (128 ×8) to be interfaced with CPU. Consider that each of the memory has two enable pins $\overline{CS_1}$ and $\overline{CS_2}$. Design the interface circuit. No explanation required.

4. Compare Harvard and modified Harvard architectures of a processor based system. Explain the working function of keypad.

5. What is device driver ? Differentiate between SRAM and DRAM.

6. Explain with suitable diagram SHARC processor.



GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Compare RISC and CISC architectures.

   b) What are the specific features of an Embedded system ?

   c) Suppose a processor's TLB (Translations Look aside Buffer) has hit-ratio of 80% and it takes 20 nanosecond to search the TLB and 100 ns to access main memory. What will be the effective access time ? 4 + 5 + 6

8. a) Discuss Embedded system development cycle.

   b) Given the following, determine the size of subfields in the address for direct mapping, associative mapping and set associative mapping cache scheme.

   We have 256 MB main memory and 1 MB cache memory. The address space of this processor is 256 MB. The block size is 128 bytes. There are 8 blocks in a cache set.

   c) Describe different components of embedded system.

   4 + 6 + 5

9. a) What are the cache replacement policies ?

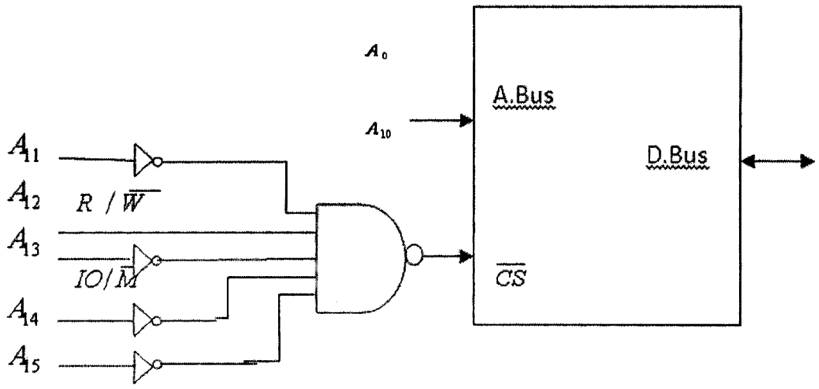
   b) Write short note on IrDA.

   c) There are 4 registers *A*, *B*, *C* & *D* each of 4-bit length. Design a circuit which could access any one of the register at a time, depending on the value of the selection line. 4 + 5 + 6

10. a) Write a short note on Bluetooth technology.

b) Distinguish between "general purpose OS" and "RTOS".

c) Given :



Find :

i) the size of the memory

ii) address length of the memory

iii) status of the CPU. 5 + 5 + 5