

Name :

Roll No. :

Invigilator's Signature :

CS/M.TECH(ECE-VLSI)/SEM-1/MVLSI-103/2011-12

2011

DIGITAL IC DESIGN

Time Allotted : 3 Hours

Full Marks : 70

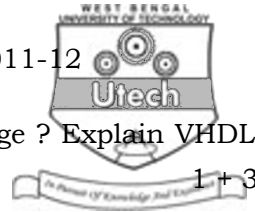
The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

*Answer Question No. **1** and any **four** from the rest.*

$$5 \times 14 = 70$$

1. a) Using a single concurrent statement, generate a symmetrical 1 MHz clock. Can it be synthesized ? 2
- b) Write the description of a CMOS inverter entity INV with a propagation delay of 10 ns. 1
- c) What are the steps performed inside a logic synthesizer for logic synthesis ? 1
- d) Compare FPGA with CPLD. 2
- e) "Punch through is an extreme case of channel length modulation." Justify. 2
- f) What are the advantages of SRAM over DRAM ? 2
- g) What is technology mapping ? 2
- h) Implement $f = \overline{a \cdot b + c}$ using Pseudo-NMOS logic. 1
- i) What are the constraints applied during logic synthesis ? 1



2. a) What is hardware description language ? Explain VHDL Design architecture. 1 + 3
- b) What are the advantages and disadvantages of VHDL ? 5
- c) Write VHDL code for a positive edge triggered *D-FF* with an asynchronous reset input (*rst*). When *rst* = 1, the output must be turned low, regardless of clock. Otherwise the output must copy the input at the moment when clock changes from 0 to 1. 5
3. a) What is high-level synthesis and what is the need for high level synthesis ? 1 + 2
- b) Explain data path synthesis and control synthesis. What is the difference between data path and controller ? 2 + 2
- c) A digital circuit can be described at gate level, behavioural level and RTL level, but RTL level is the preferred, why ? 3
- d) Draw the data flow graph for the following basic blocks : 4

$$t_1 \leq a + b;$$

$$t_2 \leq c \times t_1;$$

$$t_3 \leq d + t_2;$$

$$t_4 \leq e \times t_3;$$
4. a) Write the acronym for VHDL. What is parameterized blocks in VHDL ? 3
- b) Explain typical VHDL design flow. 3
- c) What do you understand by "PORT MAP" ? 3
- d) Write VHDL code to obtain a Full-Adder from two half-adder and an OR gate. 5



5. a) What is Binary Decision Diagram (BDD) ? How ROBDD is obtained from BDD ? Draw the ordered binary decision diagram for the function $f = (a + b) c$.

1 + 4 + 3

- b) Explain sequential logic synthesis steps. What are the two main approaches of state minimization ?

4 + 2

6. a) What is PLA ? How is PLA different from PAL ?

1 + 1

- b) Design a CMOS NOR-NOR PLA that has a , b and c as inputs and outputs the POS functions :

6

$$f_1 = (a + \bar{b} + c)(\bar{a} + b + c)$$

$$f_2 = (\bar{a} + b + \bar{c})(a + b + c)$$

$$f_3 = (a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + \bar{c})$$

- c) Design a MOSFET programmable ROM that contains the following data :

6

Address	0	1	2	3	4	5	6	7
Data	0100	1111	1010	0001	1011	0111	1110	1001

7. a) What are the goals of floor planning ? What are the constraints used in floor planning ? Differentiate between floor plan and placement. How placement algorithms are classified ?

2 + 1 + 2 + 2

- b) What is partitioning ? What are the constraints used in partitioning ? How partitioning affects delay ?

1 + 1 + 1

- c) Explain global routing. Why is the routing process divided into two phases ?

1 + 3



8. a) What are the advantages of dynamic logic over static logic ? Why dynamic logic cannot be cascaded directly ? How domino logic solves the cascading problem of dynamic logic ? Implement the logic function $f = \overline{a \cdot b + c \cdot a}$ using the smallest number of transistors using dynamic logic. 1 + 2 + 2 + 2
- b) Implement $f = a \cdot \bar{b} (c + \bar{d})$ using Pseudo-NMOS logic. 2
- c) Explain various non-ideal effects of dynamic logic circuits. 5

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