Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(ECE)/SEM-1/MVLSI-103/2010-11

2010-11

ADVANCED DIGITAL INTEGRATED CIRCUIT DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer Question No. 1 and any *four* from the rest.

1. Write *true* of *false* with proper justification : 7 × 2
   - i) SRAM is a bistable circuit.
   - ii) Bootstrap capacitance is used to remove charge sharing problem.
   - iii) Enhancement NMOS can be used as load in CMOS configuration.
   - iv) In a single HDL program both dataflow and structural and behavioural design can be used.
   - v) Zipper clock is a type of global clock.
   - vi) Simulated annealing is a type of combinational logic optimization.
   - vii) BDD is a combinational logic optimization.
2. a) Implement a 4-input decoder using VHDL.
   b) Write the difference between different design methodologies of writing HDL program.
   c) What is HDL ? 7 + 5 + 2

3. a) What is dynamic logic circuit ? Discuss its advantage and disadvantage over static logic.

   b) Calculate the time taken for the Dynamic NMOS logic'0' transfer event.

   c) Design a dynamic *D* register with single clock transmission gate logic. 4 + 5 + 5

4. a) What is cascading problem in dynamic CMOS logic circuit and how can it be removed ?

   b) Implement the following function using dynamic logic, domino logic and four phase clock.

   $F = A + B' . C + D . (A + C')$ 5 + 9

5. a) Design FSM for the following table :

Present State			***Input***	***Next State***			***Output***
	P **1**	***P*** **0**	***X***		***N*** **1**	***N*** **0**	***Z***
S_{EE} =	0	0	a = 00	S_{OE} =	1	1	p = 0
S_{EE} =	0	0	b = 01	S_{EO} =	0	1	p = 0
S_{EE} =	0	0	c = 10	S_{EE} =	0	0	p = 0
S_{EO} =	0	1	a = 00	S_{OO} =	1	0	q = 1
S_{EO} =	0	1	b = 01	S_{EE} =	0	0	q = 1
S_{EO} =	0	1	c = 10	S_{EO} =	0	1	q = 1
S_{OO} =	1	0	a = 00	S_{EO} =	0	1	p = 0

S_{OO} =	1	0	$b = 01$	S_{OE} =	1	1	$p = 0$
S_{OO} =	1	0	$c = 10$	S_{OO} =	1	0	$p = 0$
S_{OE} =	1	1	$a = 00$	S_{EE} =	0	0	$p = 0$
S_{OE} =	1	1	$b = 01$	S_{OO} =	1	0	$p = 0$
S_{OE} =	1	1	$c = 10$	S_{OE} =	1	1	$p = 0$

b) What is the difference between Moore Machine and Mealy machine ? 10 + 4

6. a) What is BDD ? How is it helpful in logic optimization ? Discuss with proper example.

b) Design layout for the following CMOS logic function.

$$F = (A . B) + C . (D + E)$$ 7 + 7

7. a) What is meant by self timed system ?

b) What is multiphase logic system ? Describe with proper example.

c) Compare between SRAM and DRAM.

d) Describe how DRAM works. 2 + 3 + 2 + 7

8. Write short notes on the following : 7 + 7

a) Flash memory

b) Genetic algorithm.