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CS/M.Tech(ECE)/VLSI/SEM-1/MVM-102/2009-10

2009

ADVANCED ANALOG INTEGRATED CIRCUIT

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Graph sheet(s) will be provided by the Institution.

GROUP – A

(Objective Type Questions)

1. Answer any *five* of the following : 5 × 2 = 10

   a) Write all the three equations of g_m and plot the graphs showing MOS transconductance as a function of overdrive and drain current.

   b) If we apply a voltage V_g at the gate of a NMOS and 1V at the source and then make drain terminal open then plot the on-resistance of NMOS as a function of V_g. Assume $\mu_n C_{ox}$ = 50 μA/V^2, $(W/L)_n$ = 10 and V_{TH} = 0·7 V.

   c) Sketch a table which includes V_{ds}, V_{gs} and I_d for four types of MOSEFETs (N-EMOS, N-DEMOS, P-EMOS and P-DEMOS).

d) What is cut-off frequency ? Derive its expression using small signal model of a NMOS.

e) For a high-pass passive RC filter, derive its gain and phase angle and plot it properly.

f) What is the caveats of Miller's theorem ? Explain it with examples.

g) What is the difference between cascade and coscode ? Give two singificant advantages of cascade over single stage amplifiers.

GROUP – B

(Long Answer Type Questions)

Answer any *five* of the following. 5 × 12 = 60

2. a) What is back gate effect ?

b) Following three figures indicate the relation between *dc* gain $A_v(0)$, bandwidth and output swing as a function of R_d and input (both *ac* and *dc*) voltages for a resistive load NMOS invereter. From these figures give some important trade-offs between *dc* gain $A_v(0)$, bandwidth and output swing and also make comments on improvement.

Dia.

c) Calculate the output voltage swing limits (for V_{dd} = 5 V), small signal *dc* gain inverter, the output resistance and the –3dB frequency of active load in Figure 2c (1) if $(W/L)_1$ = 2μm and $(W/L)_2$ = 1μm, C_{gd1} = 0·5 fF, $C_{bd1} = C_{bd2}$ = 10 fF, C_{gs2} = 2 fF, C_L = 1 pf and $I_{d1} = I_d 2$ = 100 μA, V_{T0n} = 0·7 V, V_{T0p} = – 0·7 V, K_n = 110 μA/V^2, K_p = 50 μA/V^2, γ = 0·4V$^{1/2}$ for NMOS, γ = 0·574V$^{1/2}$ for NMOS, λ = 0·04 V^{-1} for NMOS and λ = 0·05 V^{-1} for NMOS.

Dia.

Fig 2c (1) Fig 2c (2)

2 + 5 + 5

3. a) Following two figures indicate two plots of voltages and currents of an NMOS CS stage with diode connected load. Indicate the operating conditions of two NMOSs (M1 : Driver and M2 : Load) used in this cofiguration in all three regions and also comment on useful region.

dia.

b) "Necessity for higher gain makes the bias point unfavourable to ouput swing". Exlain this lemma with example for a CS stage with diode connected load.

c) The CS stage with current source (Figure 2c (2)) is called current source inverter. Why ? Then draw the schematic of current sink inverter.

d) Examine the performance of a current-source using the design equations :

$(W/L)_1 = 2\ \mu m$ and $(W/L)_2 = 1\ \mu m$, $C_{gd1} = 0{\cdot}5$ fF, $C_{bd1} = C_{bd2} = 10$ fF, $C_{gs2} = 2$ fF, $C_L = 1$ pf and rest values are taken from problem 2(c) except the value of I_{d1} and I_{d2}. What is the value of V_{GB} = to make $I_{d1} = I_{d2} = 291\ \mu A$? 3 + 3 + 3 + 3

4. a) Then derive its small signal *dc* gain and input range ΔV_{im} and draw the curve showing G_m versus $\pm \Delta V_{im}$.

b) Derive the output impedance and *dc* gain of the following circuit in figure (a).

dia.

c) Derive the low-frequency small signal gain of the source follower (SF) shown in Figure 4(a) and explain the $V_{out} - V_{in}$ plot in figure 4(a). Now justify why we switch over from the basic circuit of SF to SF using NMOS as current source in Figure 4(b).

Dia.

Figure 4(a). Figure 4(b) 4 + 4 + 4

5. a)

dia.

Figure 5(a). Figure 5(b)

In figure 5, transistor senses ΔV at the input and delivers a propotional current ($I_d = -\Delta V_{gm}$) to a 50-Ω transmission (T) line. The other end of T-line is terminated by a 50Ω resistor in Figure (a) and a common gate stage in Figure (b). $\gamma = \lambda = 0$. Then find out *dc* gain A_v (0) for both the cases and what condition is necessary to minimize reflection (wave) at source node of M1 ? Does second arrangement in Figure 5(b) provides higher gain than first one ? Justify it.

b)

dia.

Figure 5(c). Figure 5(d)

Draw the small-singal equivalent circuit of Figure 5(c). Then find out the *dc* gain of the telescopic cascade amplifier shown in Figure 5(d). Finally redraw the *ac* equivalent circuit using ideal current soure in place of M3 (Figure 5(d)). 5 + 7

6. a) Design a telescopic cascode amplifier (with PMOS current source load as in Figure 5(c)) with following specifications :

A_{vo} = – 100, P_{diss} = 1 mW, V_{OUT} (max) = 4 V,
V_{OUT} (min) = 1·5 V, C_L = 10 pF, SR > 10V/μs,
K_n = 150 μA/ V^2 , V_{TH} = 0·7, V_{DD} = 5V. Also specify maximum and minimum value of output swing.

b) The figures show the implemenatation of folded cascode from telescopic cascode. Now find out the R_{OUT} for every case and compare them considering the I_2 as NMOS current-sink or PMOS current-source. 6 + 6

Dia.

7. a) Using the material and divice parameters in Q. 2(a), design a two stage OP-AMP as shown in Figure 7(a) that meets the following specifications :

$A_v(0) > 5000$, $V_{DD} = 2{\cdot}5$ V, $V_{SS} = -2{\cdot}5$ V,

GBW = 10 MHz, $C_L = 2$ pF, SR > 10V/μs,

$V_{OUT} = (p \text{ to } p) = \pm 2$ V, ICMR = – 1V to 2 V,

$V_{diss} <= 1$mW, $V_A = 20$ V.

b) "Slew rate of 2-stage OP-AMP is limited by the first stage only". Justify it with daigram showing Miller effect. If 741 OP-AMP has a SR of 1V/μs wih V_{OUT} = (p to p) = ± 14 V, then what is maximum operating frequency for undistorted output ? 7 + 5

dia.

Figure 7(a). Figure 7(b)

8. a) Justify why a two pole system (say 2 stage Op-Amp) is unstable without compensation and why a –ve feedback system in converted into a +ve feedback system (unstable and oscillatory) ? How could we recover from here ?

b) Design the current and W/L values of the current-mirrored DE-AMP to satisfy the following specifications :
$A_v(0)$ > 100, V_{DD} = 2·5 V, V_{SS} = – 2·5 V,
SR > = 10V/μs, (C_L = 2 pF), f – 3 dB > = 10 kHz,
– 1·5 V < ICMR < 2 V, V_{diss} < = 1mW and using the material and derive parameters in Q 2(a). 7 + 5