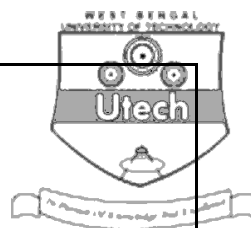
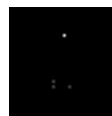
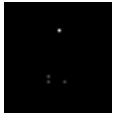


[ Full Marks : 70



**DO NOT WRITE ON THIS PAGE**



**CS/M.Tech (CSE)/SEM-2/MCS-204B/09**  
**REAL TIME & EMBEDDED SYSTEM**  
**SEMESTER - 2**



Time : 3 Hours ]

[ Full Marks : 70

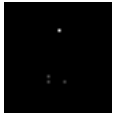
*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

Answer Question No. 1 and any *five* from the rest.

$$20 + ( 5 \times 10 ) = 70$$

1. Answer any *four* questions : 4 × 5
- a) Discuss on the key constraints related to embedded system design.
  - b) What do you mean by Hard, Firm and Soft Real Time Systems ?
  - c) What is the role of Hardware Software Co-design and Co-synthesis in embedded system design ?
  - d) Discuss on the key features of a Real-Time Operating System.
  - e) What do you mean by Interrupt Latency and Interrupt Dispatch Latency ?
  - f) What do you mean by propagation delay, hold time delay and set-up delay in logic circuits ?
2. a) Discuss with the help of a block diagram how, Closed Loop Feedback Control is used in Real-Time Systems.
- b) Critically Comment — "Real Time Systems must be responsive to events". 8 + 2

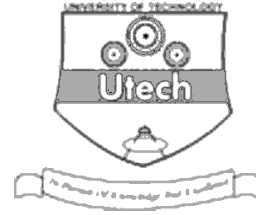


3. a) Discuss on the following terms in context to Real-Time Task Scheduling :

i) Proficient Scheduler

ii) Optimal Scheduler

iii) Jitter.



b) Discuss on the scheduling issues related to periodic tasks in contest to Real-Time Scheduling. 6 + 4

4. a) Discuss the significance of Hardware – Software Partitioning in Embedded System Development.

b) What do you mean by Simulation and Synthesis of design models ? 6 + 4

5. a) Compare between absolute deadline and relative deadline of tasks. Define response time of a task. What do you mean by task precedence ?

b) Briefly the Earlies deadline first scheduling of real-time tasks. 6 + 4

6. a) Discuss how interrupts are scheduled in a Real-Time OS.

b) Discuss on the different types of processor architecture used to build Embedded System Hardware.

c) What is the principle of storage in Flash Memory ? 3 + 5 + 2

7. a) What do you mean by entity and architecture in context to VHDL ? What is a process ? State the significance of a process in the VHDL description with a given example. What is a signal in VHDL ?

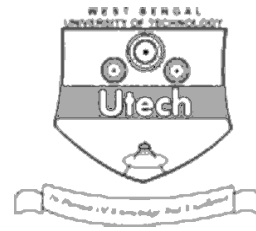
b) Discuss with an example how a sequential circuit is described in VHDL. 7 + 3



8. Write short notes on the following :

5 + 5

- a) Table Driven Scheduling
- b) Data Sharing among Tasks.



---

END