Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech (CSE)/SEM-2/CST-622/2011

2011

EMBEDDED SYSTEM AND VSLI DESIGN

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *seven* questions. 7 × 10 = 70

1. a) State the fundamental issues in hardware-software co-design.

   b) Name the area of applications for the following processors :

      i) Digital Signal Processor

      ii) Media Processor.

   c) With respect to embedded system give a simple design of a digital camera. 2 + 3 + 5

2. a) Why do you need a cross compiler ?

   b) It is required to design a Real Time Robot Control System. For this application select the appropriate processor based on :

      - Instruction cycle time
      - Bus width
      - MIPS
      - On-chip RAM/ROM/EEPROM/Flash Memory.

   c) Briefly describe the different structural units in an embedded processor. 2 + 3 + 5

3. a) Explain the significance of task scheduling in RTOS.

   b) Explain the process of converting a C-program into a file for ROM image.

   c) Three processes with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 milliseconds respectively enter the ready queue together. A new process P4 with estimated completion time 2 ms enters the ready queue after 2 ms. Assume that all the processes contain only CPU operation and no I/O operation are involved. Apply pre-emptive shortest remaining time scheduling for the above process and also calculate average turn-around time. 2 + 3 + 5

4. a) Describe the process of fabrication of NMOS transistor. Clearly illustrate the sequence of process with proper diagram.

   b) Write the advantages of ion implantation process over diffusion process. 8 + 2

5. a) Sketch the V – I curve for *n*MOSFET. Explain the different regions of operation and the parameters involved.

   b) An FET process is described by the parameters $K_n^{\prime} = 110\,\mu A/V^2$ and $V_{T0,\,n} = +\,0\cdot 7V$. The voltages are measured to be $V_{GS,\,n} = 2V$, and $V_{SB,\,n} = 0V$.

      i) A *n*FET with an aspect ratio of 4 has a drain current of 340 μA flowing through it. Find the drain to source voltage $V_{DS,\,n}$

      ii) A different FET is biased with $V_{DS,\,n} = 2V$ and $V_{SB,\,n} = 0V$. The current is measured as 440 μA. Find the gate to source voltage $V_{GS,\,n}$ if the aspect ratio is known to be 8. 4 + 3 + 3

6. a) Implement the following function using CMOS logic :

   $f(A,\,B,\,C) = A^{\prime}BC + AB^{\prime}C + ABC^{\prime}$.

   b) Explain the implementation of CMOS based D flip-flop. 4 + 6

7. a) Explain the DC characteristics of CMOS inverter with neat sketch.

b) Consider a CMOS inverter with the following parameters :

nMOS : $V_{T0,\,n} = +0 \cdot 6V$ $\mu_n C_{ox} = 60\mu A/V^2$

pMOS : $V_{T0,\,p} = -0 \cdot 7V$ $\mu_p C_{ox} = 25\mu A/V^2$

The power supply voltage is $V_{DD} = 3 \cdot 3V$. The channel length of both transistors is $L_n = L_p = 0 \cdot 8\mu m$.

i) Determine the (W_n/W_p) ratio so that the switching threshold voltage of circuit is $V_{th} = 1 \cdot 4V$.

ii) The CMOS Fabrication process used to manufacture this inverter allows a variation of the $V_{T0,\,n}$ value by ± 15% around its nominal value, and a variation of the $V_{T0,\,p}$ value by ± 20% around its nominal value. Assume that all other parameter such as $(\mu_n,\ \mu_p,\ C_{ox},\ W_n,\ W_p)$ always retain their nominal value. Find the upper and lower limits of the switching threshold voltage V_{th} of this circuit. 4 + 3 + 3

8. a) State the differences between synthesis and simulation.

b) Write the VHDL code for 4 to 1 multiplexer using data flow modelling as well as behavioural modelling. 4 + 3 + 3