

Invigilator's Signature :



- iii) Which of the following is not true about SIMD ?
- a) On a memory access, all active processors must access the *same location* in their local memory
 - b) All active processors execute the same instruction synchronously, but on different data
 - c) Consists of two types of processors
 - d) All the processing elements (PEs) execute in parallel and none of the units can be allowed to skip any particular instruction.
- iv) In distributed memory machines
- a) processors communicate by passing messages to each other
 - b) coordination of accesses to locations done by use of locks provided by thread libraries
 - c) memory is globally shared; therefore processes (threads) see single address space
 - d) each processor has its own local memory which can be accessed by others at times.

GROUP – B

(Short Answer Type Questions)

Answer *all* the following questions. $2 \times 5 = 10$

2. Flynn's taxonomy grouped computer architectures into four types on the basis of their instruction and data stream. What are they ? Describe each of them.
3. Write short notes on Grid and Cloud computing. Discuss the concept of virtualization in this context.



GROUP – C

(Long Answer Type Questions)

Answer any *four* of the following.

4 × 14 = 56

4. SIMD operations almost always use scalar arrays as input data. However, the data structure of these arrays is not always suited for SIMD operations. The built-in function `vec_perm (va, vb, vpat)` is used for vector realignment where *va* and *vb* are vectors and *vp* is the realignment pattern.
 - a) Explain with an example how this realignment works.
 - b) Write an SIMD 4×4 matrix transpose program where each element of the matrix is 4 bytes long using `vec_perm ()` function.
5.
 - a) What is multi-core architecture ? Compare multi-core and simultaneous multithreading (SMT). Explain how the two can be combined to make programs run faster.
 - b) Describe the cache coherence problem in multi-core architectures. Discuss the different techniques to solve it.
6. a) Answer the following questions given the following reservation table with a pipeline clock cycle $\tau = 20$ ns.

X					X
	X		X		
		X			
			X	X	

- i) What are the forbidden latencies and the initial collision vector ?
- ii) Draw the state transition diagram for scheduling the pipeline.
- iii) Determine the MAL.

8



- b) Suppose an operation can be subdivided into 6 sub-operations.

A 6-stage pipeline is implemented with the stages consuming the following execution times : 130, 90, 180, 100, 120 and 80 picoseconds. What is the clock period of the pipeline ?

Suppose pipelining introduces an overhead of 20 ps. What is the maximum speed-up achievable in this system ?

7. a) Describe the difference between RISC and CISC architectures. 4
- b) Design a data path for MIPS architecture for
- i) ADD/SUBTRACT
- ii) LOAD/STORE instructions. 10
8. a) What is the difference between a vector processor and a parallel processor ? 3
- b) Explain with diagram how a vector processor speeds up vector operation. 6
- c) What is chaining and scatter/gather operation in Vector processor ? 5
9. a) What are the different types of data hazards encountered in pipelining ? 3
- b) How are RAW hazards solved in pipelining ? 4
- c) Explain with state diagram the technique of Dynamic Branch Prediction in pipelining. 7
-