

CS / M.Tech (CSE) / SEM-2 / CSEM-202 / 09
ADVANCED COMPUTER ARCHITECTURE (SEMESTER - 2)



1.
Signature of Invigilator

2.
Signature of the Officer-in-Charge

Reg. No.

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Roll No. of the
Candidate

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CS / M.Tech (CSE) / SEM-2 / CSEM-202 / 09
ENGINEERING & MANAGEMENT EXAMINATIONS, JULY - 2009
ADVANCED COMPUTER ARCHITECTURE (SEMESTER - 2)

Time : 3 Hours]

[Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **36 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
b) For **Groups – B & C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

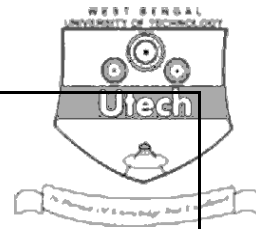
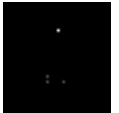
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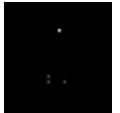
	Group – A										Group – B										Group – C										Total Marks	Examiner's Signature
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Head-Examiner / Co-Ordinator / Scrutineer

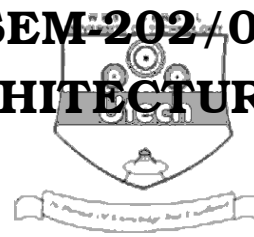
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SEMESTER - 2



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GROUP – A**(Multiple Choice Type Questions)**

1. Choose the correct alternatives for the following :

10 × 1 = 10

i) A static pipeline processor is

a) Unifunctional

b) Multifunctional

c) Both (a) and (b)

d) None of these.

ii) The maximum speed up factor of a linear pipeline processor is

a) number of tasks processed

b) number of pipeline stages

c) infinity

d) clock period of the processor.

iii) Pipelining uses

a) Data Parallelism

b) Temporal Parallelism

c) Spatial Parallelism

d) None of them.

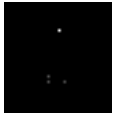
iv) Latency Values must be

a) Negative

b) Positive

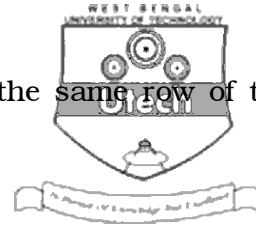
c) Either (a) or (b)

d) None of these.



v) Forbidden latency means

- a) distance between any two checkmarks in the same row of the reservation table
- b) distance between any two checkmarks in the same column of the reservation table
- c) distance between all the checkmarks
- d) none of these.



vi) The maximum latency in a K -dimensional hypercube network with N number of nodes is

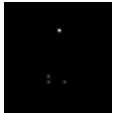
- a) N
- b) K
- c) $\log_2 K$
- d) 2^K

vii) For any statically configured pipelining the minimum value of MAL is

- a) maximum number of marks in any single row of the reservation table
- b) minimum number of marks in any single row of the reservation table
- c) number of 1's in the initial collision vector
- d) number of 0's in the initial collision vector.

viii) In hypercube interconnection network packets are forwarded along k^{th} direction if the source and destination address (Binary)

- a) differ at k^{th} position
- b) same at k^{th} position
- c) differ at $(k - 1)^{th}$ position
- d) same at $(k - 1)^{th}$ position.



ix) Scoreboarding Technique

- a) is a dynamic scheduling
- b) is a static scheduling
- c) does not allow out of order execution
- d) none of these.



x) In Tightly coupled system processors

- a) share a common clock
- b) share a common memory
- c) share a common clock or memory
- d) neither share a common clock nor a common memory.

GROUP – B

Answer any *four* of the following.

$$4 \times 5 = 20$$

2. Prove that the average latency of any greedy simple cycle is less than or equal to the number of 1's in the initial collision vector. 5
3. What is the execution time of the following instruction sequence on a 7 stage pipeline with 5 cycle instruction latency for non-branch instructions and 7 cycles for branch instructions ? Assume that the branch is not taken :

BNE R4,#0,R5

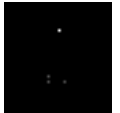
DIV R12,R1,R7

ADD R8,R9,R10

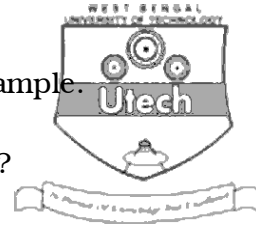
SUB R5,R12,R9

MUL R10,R5,R8.

5



4. a) Explain load-use and define-use dependency. 2
- b) What do you mean by anti-dependency ? Give example. 3
5. a) What do you mean by control dependency graph ? 2
- b) Draw the control dependency graph for the following code : 3



```

I0:  R1 = OP1
I1:  R2 = OP2
I2:  R3 = OP3
I3:  if ( R2 > R1 )
I4:      if (R3 > R1 )
I5:          R4 = R3
I6:      else R4 = R1
I7:  else R4 = R2
I8:  R5 = R4 * R4.

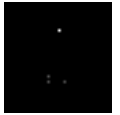
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6. a) What is WAW hazard ? 1
- b) Is WAW hazard has any effect on pipelining scheduling ? Explain with example. 4
7. How long would the following sequence of instructions take to execute on an out-of-order processor with two execution units, each of which can execute any instruction ? Consider that load operations have a latency of three cycles and all other operations have a latency of two cycles. Assume that the pipeline has 5 stages.

```

LD    R1,R2
ADD   R3,R1,R4
SUB   R5,R6,R7
MUL   R8,R9,R10
DIV   R11,R5,R8.

```



GROUP – C

Answer any *two* of the following. $2 \times 20 = 40$

8. a) Explain with example how branch instruction can create hazard in pipelining. 4
- b) Draw the state transition diagram for 2-bit prediction scheme. 2
- c) Explain with example the advantages of 2-bit prediction scheme over 1-bit prediction scheme. 4
- d) Compute the execution time of the following instruction sequence on a 5 stage pipeline with an instruction latency of 3 cycles for non-branch instruction and 5 cycles for branch instruction. Then find the reordering of instructions that gives the shortest execution time.

MUL R10,R11,R12

SUB R8,R10,R15

ADD R13,R14,R0

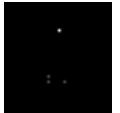
DIV R15,R2,R3

OR R7,R5,R6.

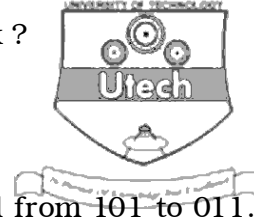
Also draw the space time diagram for both the cases.

 $2 + 4 + 2 + 2$

9. a) Draw the diagram for 2-D mesh with 9 nodes. 2
- b) Consider a $|N \times |N$ 2-D Mesh. Now answer the following : 6×1
- What is the total number of nodes in the network ?
 - What is the total number of edges in the network ?
 - What is/are the degree of the nodes in the network ?
 - What is the diameter of the network ?
 - What is the bisectional width of the network ?
 - Whether the network is symmetric or not ?



- c) Draw the 4-Dimensional Hypercube interconnection network. How the nodes are connected in this type of interconnection network ? 3 + 1
- d) Draw the Baseline Network with 8 nodes. 3
- e) Is this a blocking network ? Explain. 1 + 1
- f) Show the routing path from node 001 to 110 and from 101 to 011. $1\frac{1}{2} + 1\frac{1}{2}$



10. Consider the following reservation tables :

	0	1	2	3	4	5	6	7
1	X	X					X	X
2			X		X			
3				X		X		

Reservation table for function X

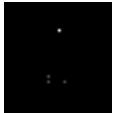
	0	1	2	3	4	5	6
1			Y		Y		
2		Y		Y		Y	
3	Y		Y				Y

Reservation table for function Y

- a) Calculate the initial collision matrices. 4
- b) Draw the modified state diagram for dynamically scheduling of above two functions. 16
11. a) Write the procedure for generating state diagram. 3
- b) Consider the following reservation table :

	1	2	3	4	5	6	7
S1	X					X	
S2			X				X
S3		X		X			
S4			X		X		

- i) Find out collision vector. 2
- ii) Draw the modified state diagram. 3
- iii) Find out all greedy cycles. 2
- iv) Calculate the MAL. 2



c) Explain the role of delay slot for handling control hazard.

4

d) Consider the following instruction sequence :

MUL R3,R4,R5

SUB R1,R2,R4

ADD R2,R1,R6

BEZ TAR

DIV R7,R8,R9.

•

•

•

•

TAR ADD R1,R2,R3



Reschedule the above code for a compiler that uses a delay slot of size three.

4

END