



Name :

Roll No. :

Invigilator's Signature :

CS/M.Tech (CSE)/SEM-2/PGCSE-204-A/2013

2013

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

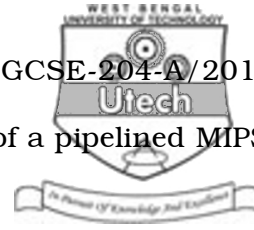
Answer Question No. **1** and any *five* from the rest.

1. Answer any *ten* of the following briefly : $10 \times 2 = 20$

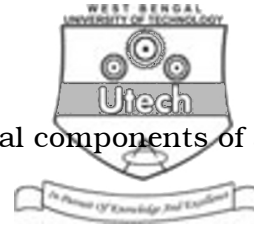
- i) Compare and contrast between byte addressing and word addressing.
- ii) Critically comment : "In MIPS architecture arithmetic operands are registers, not memory".
- iii) With proper example brief on the role of "zero" register in MIPS processor.
- iv) Critically comment : "Assembly can provide pseudo instructions".
- v) With proper example show the operation of "beq" in MIPS.



- vi) Define the term “CPU time” for a given instance of a program.
 - vii) Explain the role of state registers between the pipeline stages.
 - viii) Explain the difficulty faced in increasing the clock speed of processors to enhance their performance.
 - ix) What do you mean by dynamic and static power of hardware circuits ?
 - x) State the key difference between vector-register processors and memory-memory vector processors.
 - xi) What do you mean by dual-port memory ?
 - xii) What do you mean by space power trade-off in modern processor architectures ?
2. a) Discuss in brief on the ‘R-Type’, ‘I-Type’ and ‘J-Type’ instructions of MIPS processor.
- b) With proper example show how a 32 bit constant can be loaded into an MIPS register. 7 + 3
3. Discuss briefly with suitable examples the various addressing modes available in an MIPS processor. 10



4. a) Briefly describe the key components of a pipelined MIPS data path.
- b) State any *two* advantages of pipelined MIPS data path over single cycle MIPS data path. 8 + 2
5. a) What do you mean by structural hazard in a pipelined architecture ? State the probable causes of structural hazard and their respective measures as practised in a pipelined MIPS architecture.
- b) State the probable causes of data hazard in a pipelined MIPS architecture. (2 + 4) + 4
6. a) Discuss briefly with proper examples the following data dependencies as found between the code instructions :
- i) Read after Write
- ii) Write after Read
- iii) Write after Write.
- b) State with proper example how loop unrolling helps to increase the throughput of a processor. 3 + 7



7. a) Discuss briefly on the key architectural components of a vector processor.
- b) What do you mean by 'stride' ? State its use in vector processor. 5 + 5
8. a) Discuss with proper illustrations the arrangement of the cores in a multi-core CPU chip.
- b) Compare the features of multi-core processor architecture with SMT processors. 4 + 6
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