Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.TECH(CSE)/SEM-2/PGCS-202/2010

2010

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Very Short Answer Type Questions)

Answer any *five* of the following : 5 × 2 = 10

1. What is latency cycle ?
2. What do you mean by speed-up of the pipeline ?
3. What is the optimal throughput of the pipeline ?
4. What is the difference between tightly coupled and loosely coupled systems ?
5. What do you mean by static pipelining ?
6. What is greedy cycle ?
7. What is the difference between multiprocessor and multi-computer systems ? 2

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

8. a) What do you mean by multiprocessor system ? 2

   b) How many number of 2 × 2 switches and how many number of stages are required to design an $n \times n$ omega network ? 3

9. Identify all of the RAW, WAR and WAW hazards in the following instruction sequence :

   DIV R1, R2, R3

   SUB R4, R1, R5

   ASH R2, R6, R7

   MULT R8, R4, R2

   BEQ R9, # 0, R10

   OR R3, R11, R1.

   Also identify all of the control hazards in the sequence.

10. Describe how the branch type instructions can cause the damage in the performance of an instruction pipeline. What will be the solution for this ?

11. Describe the following networks : $2\frac{1}{2} + 2\frac{1}{2}$

    a) Cross-bar network

    b) Multi-port network.

12. When executing a particular program, machine *A* gives 90 MIPS and machine *B* gives 70 MIPS. However, machine *A* executes the program in 50 seconds and machine *B* executes in 40 seconds. Give the reason.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

13. Consider the following pipelined processor with 3 stages :

Dia.

a) Draw the reservation tables of the functions *X* and *Y*. 4

b) What are the forbidden latencies and the initial collision vectors ? 3

c) Draw the state transition diagram for scheduling the pipeline. 4

d) Determine the MAL associated with the shortest greedy cycle. 4

14. a) What do you mean by cache coherence problem ? What are the different protocols to solve the cache coherence problem ? Briefly discuss each of them. 8

b) Compare between centralized and distributed architectures. Which is the best architecture among them and why ? 4

c) Explain how an unauthorized access to a memory module can be prevented in multi-port networks. 3

15. Consider the three-stage pipelined processor specified by the following reservation table :

Time/stages	1	2	3	4	5
S1	×				×
S2		×		×	
S3			×	×	

a) What are the forbidden latencies and the initial collision vector ? 3

b) Draw the state transition diagram for scheduling the pipeline. 3

c) Determine the MAL associated with the shortest greedy cycle. 3

d) Determine the lower bound on the MAL for this pipeline. Have you obtained the optimal latency from the above state diagram ? 6

16. Write short notes on any *three* of the following : 3 × 5

a) Pipeline hazard detection and resolutions

b) Cube-connected network

c) Benes Network

d) Neuro-computing Architecture.

e) RISC Philosophy.