Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/M.Tech(CSE)/SEM-1/MCSE-103/2011-12

2011

PROCESSOR ARCHITECTURE & ORGANIZATION

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Answer any *ten* questions.

1. a) How many 128 × 16 RAM chips are needed to construct a memory capacity of 4096 words (16 bit is one word) ? How many lines of the address bus must be used to access a memory of 4096 words ? For chip select how many lines must be decoded ?

   b) What are the difference between Von Neumann architecture and Harvard architecture ? 5 + 2

2. a) Explain the memory hierarchy pyramid showing both primary and secondary memory in the diagram and also explain the relationship of cost, speed and capacity.

   b) Why cache memory plays an important role in memory hierarchy and show how Locality of Reference is manifested in cache operation ? 5 + 2

3. a) Explain with an example how logical address space is converted to physical address space in virtual memory ?

   b) Define page fault ? 5 + 2

4. Show the bus connection with a CPU to connect 4 RAM chips of size 256 × 8 bits each and 4 ROM chip of 512 × 8 bit each in size. Assume that the CPU has 8 bit data bus and 16 bit address bus. Clearly specify generation of chip select signals. 7

5. Briefly explain the two write policies for cache design. Compare the advantages and disadvantages of both. 7

6. According to the following information determine the size of the subfields in Direct mapped, associative cache and set associative cache.

   ✳ We have 256 MB main memory and 1 MB cache memory

   ✳ The address space of the processor is 256 MB

   ✳ The block size is 128 bytes.

   ✳ There are 8 blocks in a cache set. 7

7. a) A register is connected to a bus. Data can flow into the register and out of the register.

   Describe how you would control or "gate" the input and output.

   b) Write the steps for instruction fetch as well as execution for the following :

   Read the content of the memory location whose address is in register R1. Fetch the memory content and store in register R2.

   Draw the bus diagram also. 3 + 3 + 1

8. Control signal Cin is required to be generated at following :

   ✳ Step 2 of instruction *A*

   ✳ Step 3 of instruction *B* when $N = 0$

   ✳ Step 4 of instruction *B* when $N = 1$

   ✳ Step 5 of instruction *C*

   a) Draw the hardwired control circuit to generate the signal Cin.

   b) Write the Boolean expression for the same. 5 + 2

9. a) Explain Half Adder with logic diagram and equation.

   b) How a Full Adder can be generated with Half Adders ?

   4 + 3

10. We ant to add two floating point numbers *A* and *B*. Before sending them to the Adder, what are the processing necessary ? Explain with diagram. 7

11. How does Booth's algorithm help in multiplication ? Explain briefly with suitable example of a multiplier. Will the algorithm be always useful ? 5 + 2

12. Explain with block diagram the function of

    a) Control step counter wit step decoder

    b) Instruction Decoder

    c) Ultimately what are they used for ? 3 + 2 + 2

13. a) One of inputs to ALU is taken through a register whereas the other input is taken directly from the bus. Why ?

    b) Will there be any change if multiple buses are used ? How will multiple buses improve CPU performance ? Explain for 3 buses. 3 + 4

14. Draw the block diagram of a 4 bit binary Adder-Subtractor and mention the various inputs and outputs in the same. Use 2's complement for subtraction. 7